UNITED STATES DISTRICT COURT
WESTERN DISTRICT OF NEW YORK

| | | |
|---|---|---|
| EASTMAN KODAK COMPANY, | ) | Civil Action |
| Plaintiff, | ) | No. _____ |
| vs. | ) | |
| APPLE INC. | ) | |
| Defendant. | ) | JURY TRIAL DEMANDED |
| _____ | ) | |

**COMPLAINT AND JURY CLAIM**

1. This action arises under the patent laws of the United States, Title 35 of the United States Code, and relates to U.S. Patent No. 6,292,218 and U.S. Patent No. 5,493,335.

**The Parties**

2. Plaintiff Eastman Kodak Company ("Kodak") is a New Jersey corporation with its principal place of business at 343 State Street, Rochester, New York 14650.

3. The Defendant is Apple Inc. ("Apple"). Apple Inc., is a California corporation having its principle place of business at 1 Infinite Loop, Cupertino, California 95014. Among other things, Apple designs, manufactures, markets and sells mobile devices, including in this District and elsewhere in the United States.

**Jurisdiction and Venue**

4. This Court has subject matter jurisdiction pursuant to 28 U.S.C. § 1338 (a).

5. The personal jurisdiction of this Court over Apple is proper because Apple commits acts of infringement in violation of 35 U.S.C. § 271 and places infringing products into the stream of commerce, via an established distribution channel, with the knowledge and/or

understanding that such products are sold in the State of New York, including in this District. These acts cause injury to Kodak within the District. Upon information and belief, Apple derives substantial revenue from the sale of infringing products distributed within the District, and/or expects or should reasonably expect its actions to have consequences within the District and derives substantial revenue from interstate and international commerce. In addition, Apple has, and continues to, knowingly induce infringement within this State and within this District by contracting with others to market and sell infringing products with the knowledge and intent to facilitate infringing sales of the products by others within this District, by creating and/or disseminating user manuals for the products with like knowledge and intent, and by warranting the products sold by others within the District.

6. Venue is proper in this District under 28 U.S.C. §§ 1391 (b), (c) and 1400 (b).

**First Claim for Relief**
**(Patent Infringement)**

7. Kodak is the owner by assignment of U.S. Patent No. 6,292,218 ("the '218 patent"), entitled "Electronic Camera for Initiating Capture of Still Images while Previewing Motion Images," a true copy of which is attached hereto as Exhibit A. The '218 patent was duly and legally issued on September 18, 2001.

8. Apple has infringed and continues to infringe the '218 patent, by using, selling and/or offering to sell, within the United States, and/or by importing into the United States, products, including, but not limited to, the iPhone 3GS mobile device, which embody and/or practice Claims 15, 23, 25, 26 and 27 of the '218 patent in violation of 35 U.S.C. § 271.

9. Apple has induced, and continues to induce, others to infringe the '218 patent in violation of 35 U.S.C § 271, by taking active steps to encourage and facilitate others' direct infringement of Claims 15, 23, 25, 26 and 27 of the '218 patent with knowledge of that

infringement, such as, upon information and belief, by contracting for the distribution of the infringing mobile devices for infringing sale such as by retail sales outlets, by marketing the infringing mobile devices, by creating and/or distributing user manuals for the infringing mobile devices, and by supplying warranty coverage for the infringing mobile devices sold in this State and in this District.

10. Apple has contributorily infringed the '218 patent in violation of 35 U.S.C. § 271, by selling within the United States, offering for sale within the United States, and/or importing components that embody a material part of the inventions described in Claims 15, 23, 25, 26 and 27 of the '218 patent, are known by Apple to be especially made or specially adapted for use in infringement of Claims 15, 23, 25, 26 and 27 of the '218 patent, and are not staple articles or commodities suitable for substantial, non-infringing use, including certain mobile devices and non-staple constituent parts of those mobile devices.

11. Kodak will have put Apple on notice of the '218 patent and Apple's infringement thereof by no later than upon service this Complaint. Moreover, upon information and belief, Apple had actual knowledge of the '218 patent in advance of the filing of this complaint.

12. As a result of Apple's infringement, Kodak has suffered, and will continue to suffer, substantial damages. Kodak will also suffer irreparable harm unless Apple's infringement is enjoined by this Court.

**Second Claim for Relief**
**(Patent Infringement)**

13. Kodak is the owner by assignment of U.S. Patent No. 5,493,335 ("the '335 patent"), entitled "Single Sensor Color Camera with User Selectable Image Record Size," a true copy of which is attached hereto as Exhibit B. The '335 patent was duly and legally issued on February 20, 1996.

14. Apple has infringed and continues to infringe the '335 patent, by using, selling and/or offering to sell, within the United States, and/or by importing into the United States, products, including, but not limited to, the iPhone 3GS mobile device, which embody and/or practice Claim 1 of the '335 patent in violation of 35 U.S.C. § 271.

15. Apple has induced, and continues to induce, others to infringe the '335 patent in violation of 35 U.S.C § 271, by taking active steps to encourage and facilitate others' direct infringement of Claim 1 of the '335 patent with knowledge of that infringement, such as, upon information and belief, by contracting for the distribution of the infringing mobile devices for infringing sale such as by retail sales outlets, by marketing the infringing mobile devices, by creating and/or distributing user manuals for the infringing mobile devices, and by supplying warranty coverage for the infringing mobile devices sold in this State and in this District.

16. Apple has contributorily infringed the '335 patent in violation of 35 U.S.C. § 271, by selling within the United States, offering for sale within the United States, and/or importing components that embody a material part of the inventions described in Claim 1 of the '335 patent, are known by Apple to be especially made or specially adapted for use in infringement of Claim 1 of the '335 patent, and are not staple articles or commodities suitable for substantial, non-infringing use, including certain mobile devices and non-staple constituent parts of those mobile devices.

17. Kodak will have put Apple on notice of the '335 patent and Apple's infringement thereof by no later than upon service this Complaint. Moreover, upon information and belief, Apple had actual knowledge of the '335 patent in advance of the filing of this complaint.

18. As a result of Apple's infringement, Kodak has suffered, and will continue to suffer, substantial damages. Kodak will also suffer irreparable harm unless Apple's

infringement is enjoined by this Court.

**WHEREFORE,** Kodak requests that the Court:

1. Adjudge that Apple has infringed and continues to infringe the asserted claims of the '218 and '335 patents;

2. Preliminarily and permanently enjoin Apple from further infringement of the '218 and '335 patents;

3. Award Kodak compensatory damages;

4. Award Kodak enhanced damages of treble its actual damages for willful infringement;

5. Award Kodak its costs and reasonable experts' fees and attorneys' fees; and

6. Award Kodak such other relief as the Court deems just and proper.

**PLAINTIFF CLAIMS A TRIAL BY JURY ON ALL ISSUES SO TRIABLE.**

EASTMAN KODAK COMPANY

By its attorneys,

**HARRIS BEACH PLLC**

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# EXHIBIT A: U.S. PATENT 6,292,218

US006292218B1

(12) **United States Patent**
**Parulski et al.**

(10) **Patent No.: US 6,292,218 B1**
(45) **Date of Patent: *Sep. 18, 2001**

(54) **ELECTRONIC CAMERA FOR INITIATING CAPTURE OF STILL IMAGES WHILE PREVIEWING MOTION IMAGES**

(75) Inventors: **Kenneth A. Parulski**, Rochester; **Timothy J. Tredwell**, Fairport, both of NY (US)

(73) Assignee: **Eastman Kodak Company**, Rochester, NY (US)

( * ) Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **08/895,094**

(22) Filed: **Jul. 16, 1997**

**Related U.S. Application Data**

(62) Division of application No. 08/367,399, filed on Dec. 30, 1994.

(51) **Int. Cl.**[7] ..... **H04N 5/225**; H04N 5/222

(52) **U.S. Cl.** ..... **348/220**; 348/333.11

(58) **Field of Search** ..... 348/220, 221, 348/222, 333, 321, 223, 333.11, 333.12

(56) **References Cited**

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| 5,452,017 | * | 9/1995 | Hickman | 348/646 |
| 5,493,335 | * | 2/1996 | Parulski et al. | 348/233 |
| 5,828,406 | * | 10/1998 | Parulski et al. | 348/220 |
| 5,923,816 | * | 7/1999 | Ueda | 348/220 |

* cited by examiner

*Primary Examiner*—Wendy R. Garber
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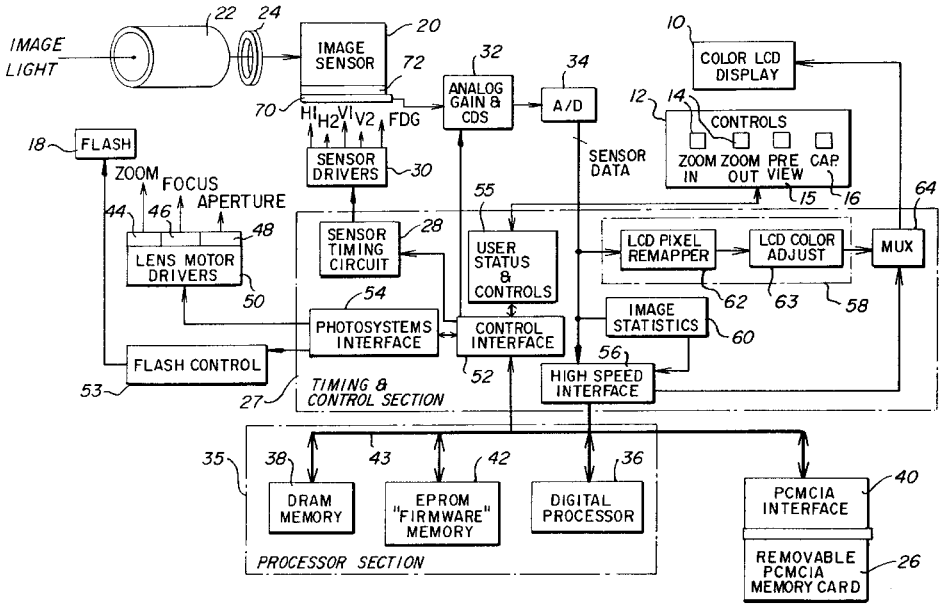
(74) *Attorney, Agent, or Firm*—Pamela R. Crocker

(57) **ABSTRACT**

An electronic camera uses a relatively more complex digital image processing technique in a still image mode to produce high quality still images, and a relatively more simple image processing technique in a motion preview mode to produce preview images of acceptable quality prior to initiation of the still image mode. The more complex digital technique is done in software in a general purpose processor section **35**, while the more simple digital technique is implemented in a fixed digital circuit in an application specific integrated circuit **27**, which also implements timing and control functions. The motion preview mode uses a shorter image readout period than the still mode and further involves mapping image sensor pixels into a fewer number of color display pixels on a color LCD display **10**. The mapping further converts color pixel signals from a mosaic array into a different color pattern on the color LCD display **10**.

**28 Claims, 10 Drawing Sheets**



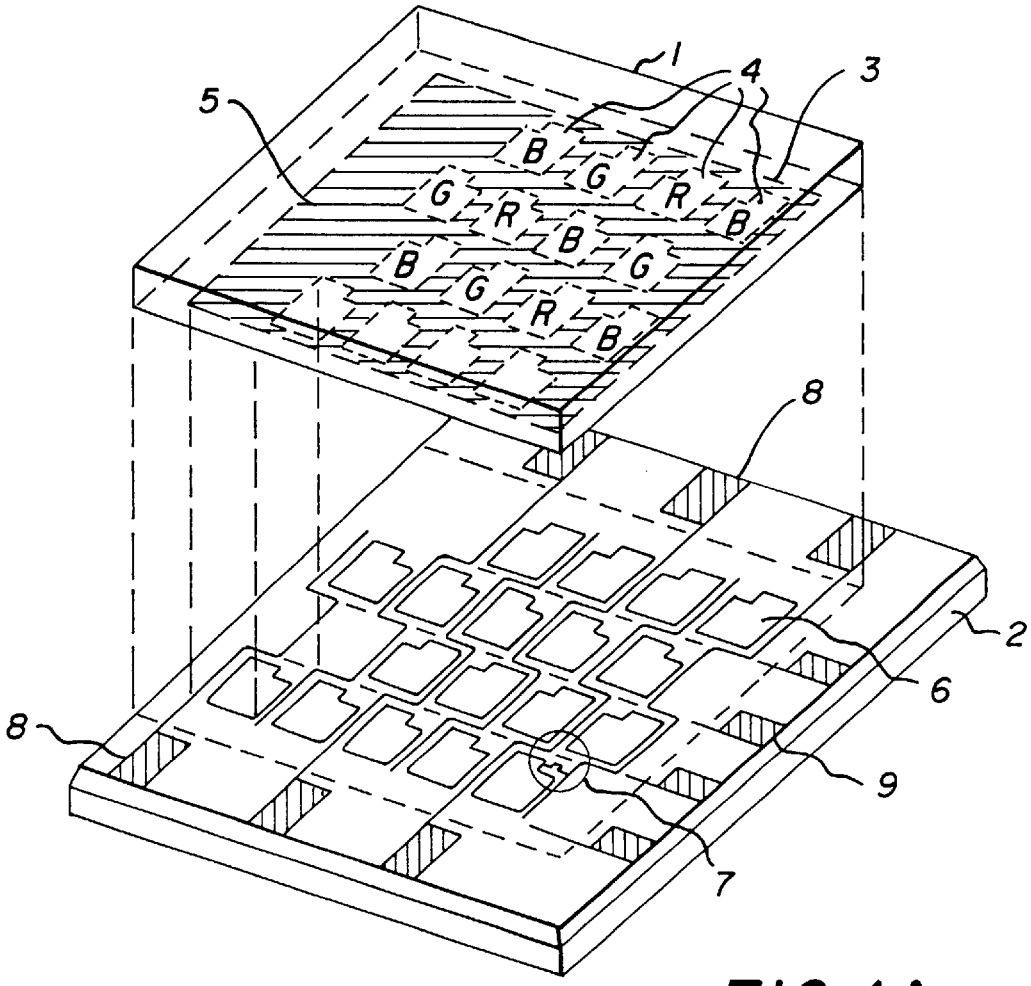



FIG. 1A

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| G | R | B | G | R | B | G | R |
| B | G | R | B | G | R | B | G |
| R | B | G | R | B | G | R | B |
| G | R | B | G | R | B | G | R |

FIG. 1B

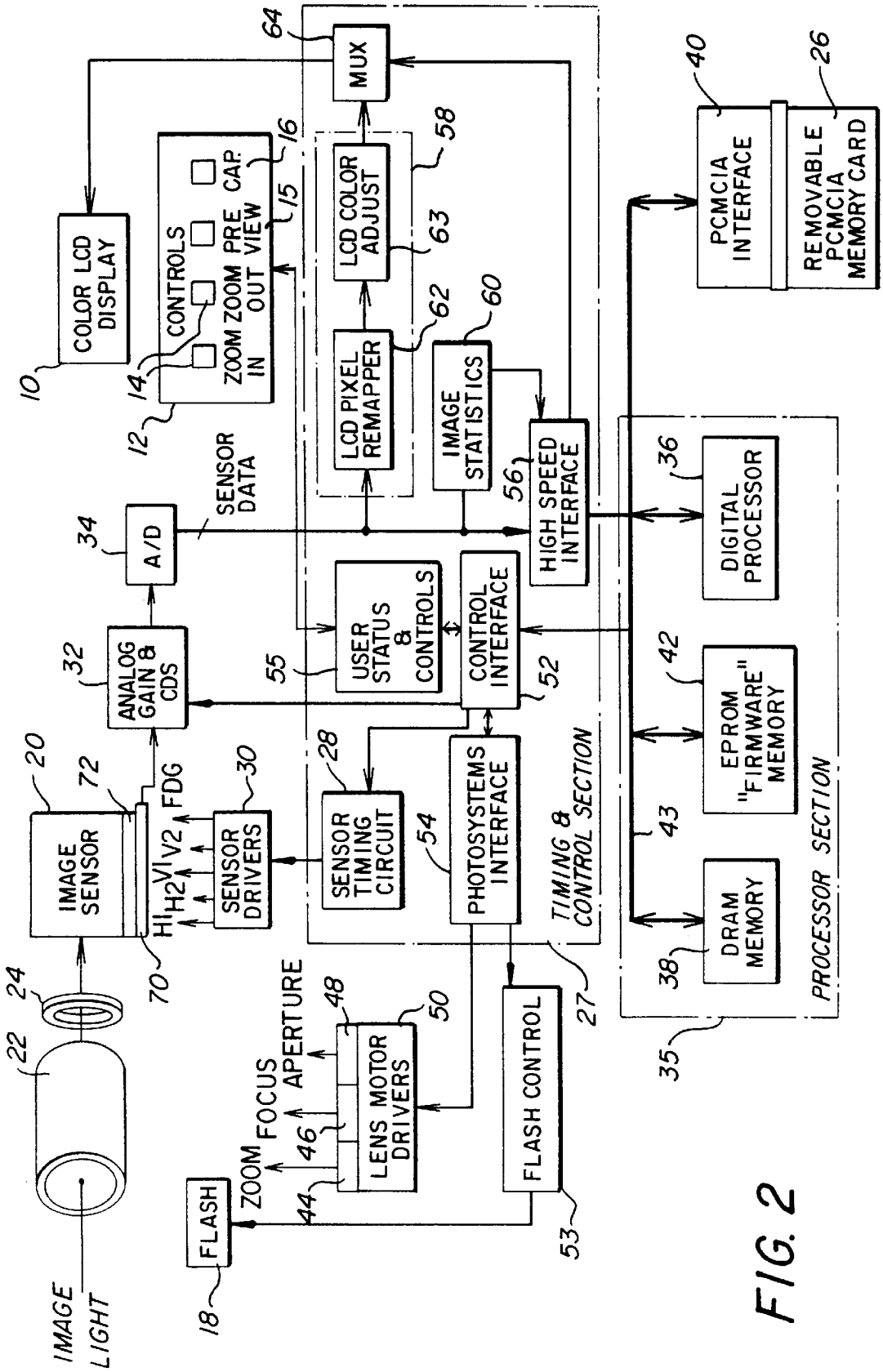


IMAGE LIGHT
LENS
APERTURE
FOCUS
ZOOM
FLASH
IMAGE SENSOR
SENSOR DRIVERS
FDG
H1 H2 V1 V2
ANALOG GAIN & CDS
A/D
SENSOR DATA
SENSOR TIMING CIRCUIT
PHOTOSYSTEMS INTERFACE
TIMING & CONTROL SECTION
LENS MOTOR DRIVERS
FLASH CONTROL
USER STATUS & CONTROLS
CONTROL INTERFACE
LCD PIXEL REMAPPER
LCD COLOR ADJUST
IMAGE STATISTICS
HIGH SPEED INTERFACE
MUX
COLOR LCD DISPLAY
CONTROLS
ZOOM IN
ZOOM OUT
PRE VIEW
CAP.
DIGITAL PROCESSOR
DRAM MEMORY
EPROM "FIRMWARE" MEMORY
PROCESSOR SECTION
PCMCIA INTERFACE
REMOVABLE PCMCIA MEMORY CARD

FIG. 2

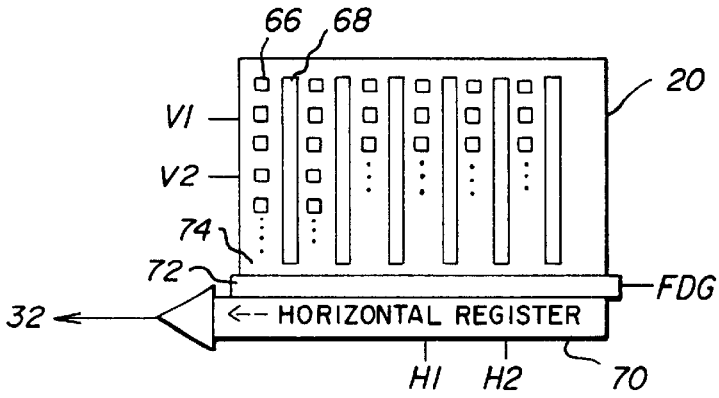



FIG. 3A

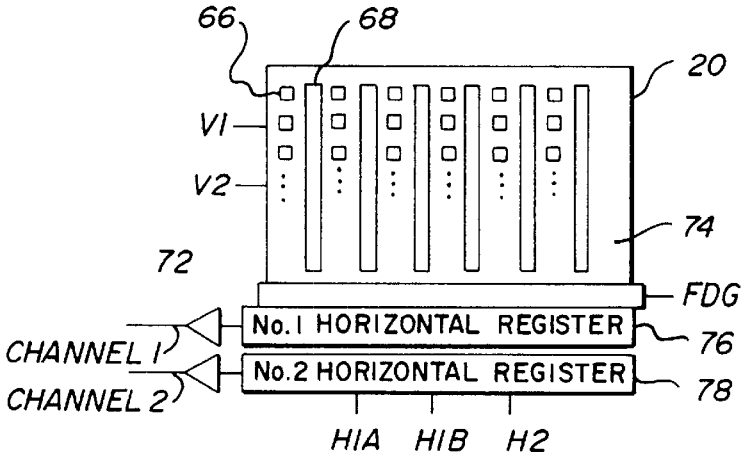



FIG. 3B

CCD LINES

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| LINE 1 | G | R | G | R | G | R | G | R |
| LINE 2 | B | G | B | G | B | G | B | G |
| LINE 3 | G | R | G | R | G | R | G | R |
| LINE 4 | B | G | B | G | B | G | B | G |
| LINE 5 | G | R | G | R | G | R | G | R |
| LINE 6 | B | G | B | G | B | G | B | G |
| LINE 7 | G | R | G | R | G | R | G | R |
| LINE 8 | B | G | B | G | B | G | B | G |

FIG. 4

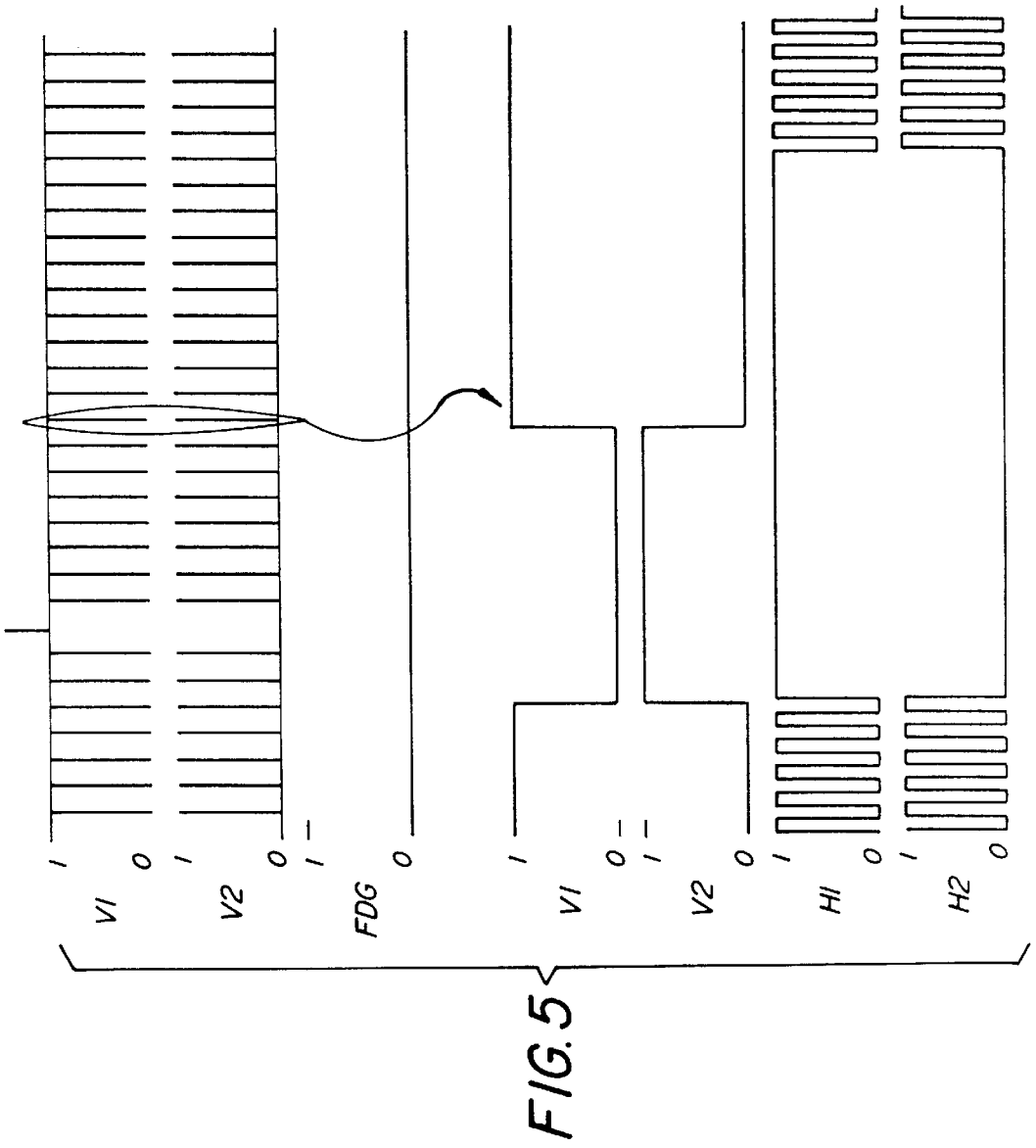



FIG. 5

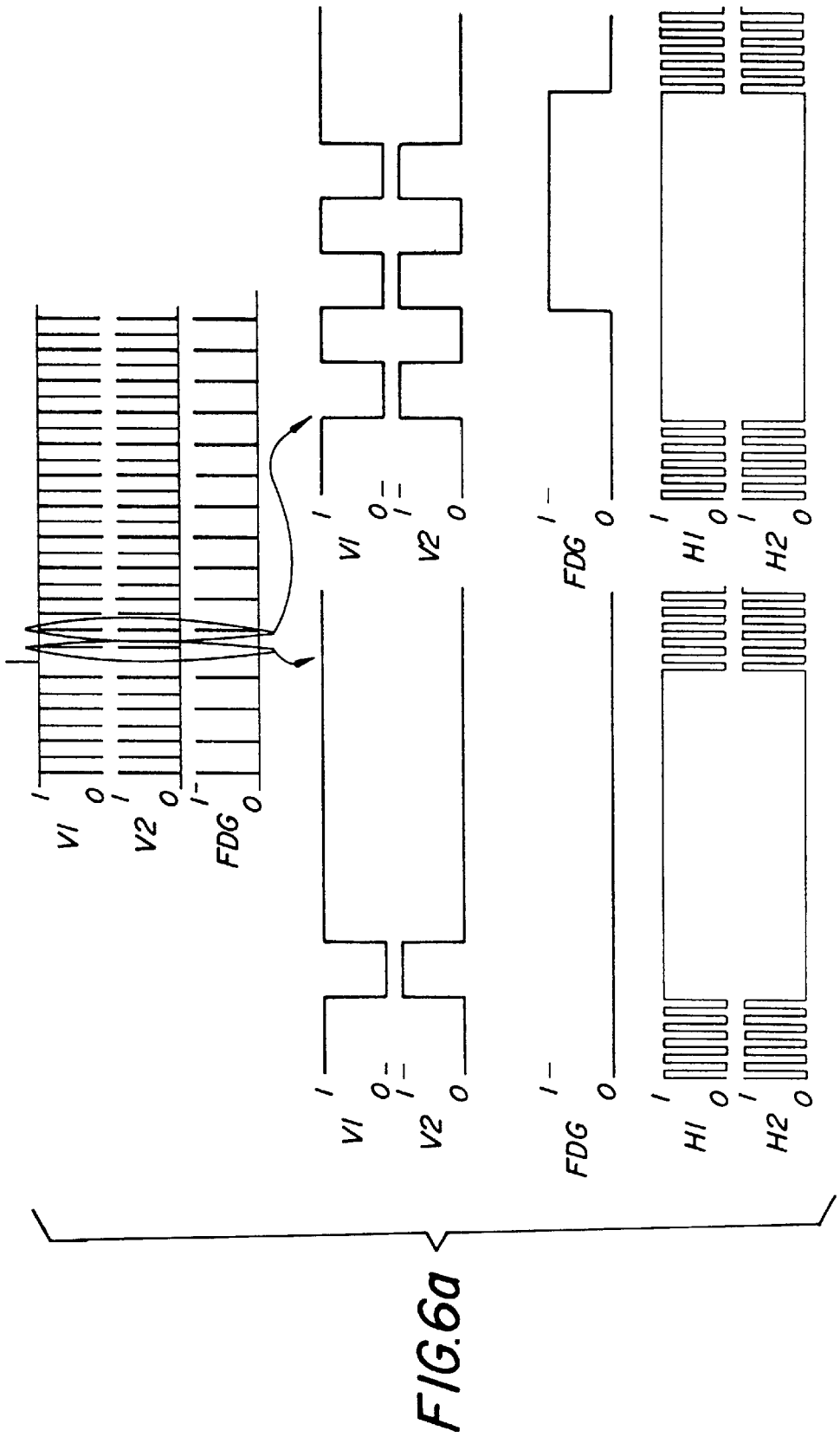



FIG.6a

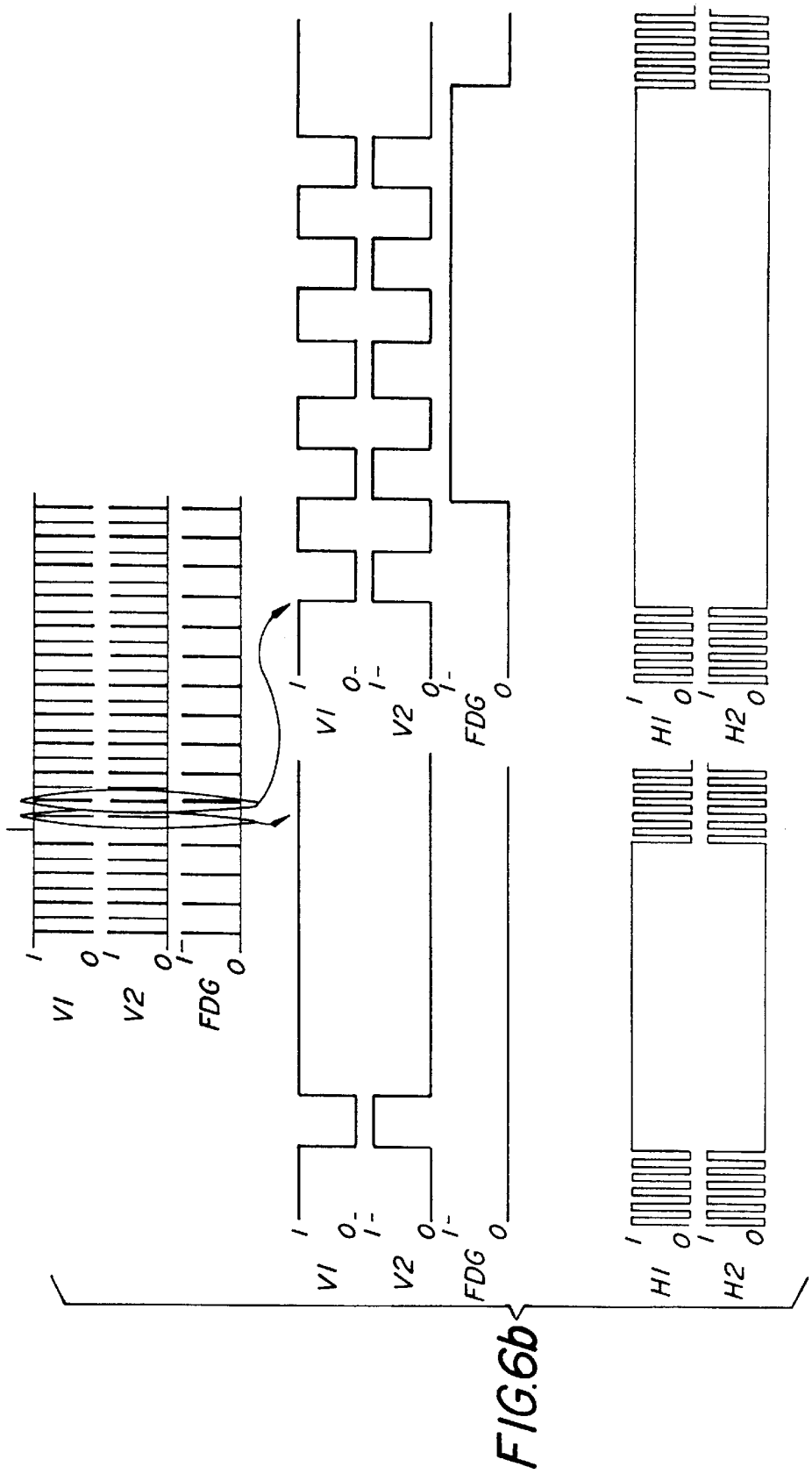



FIG.6b

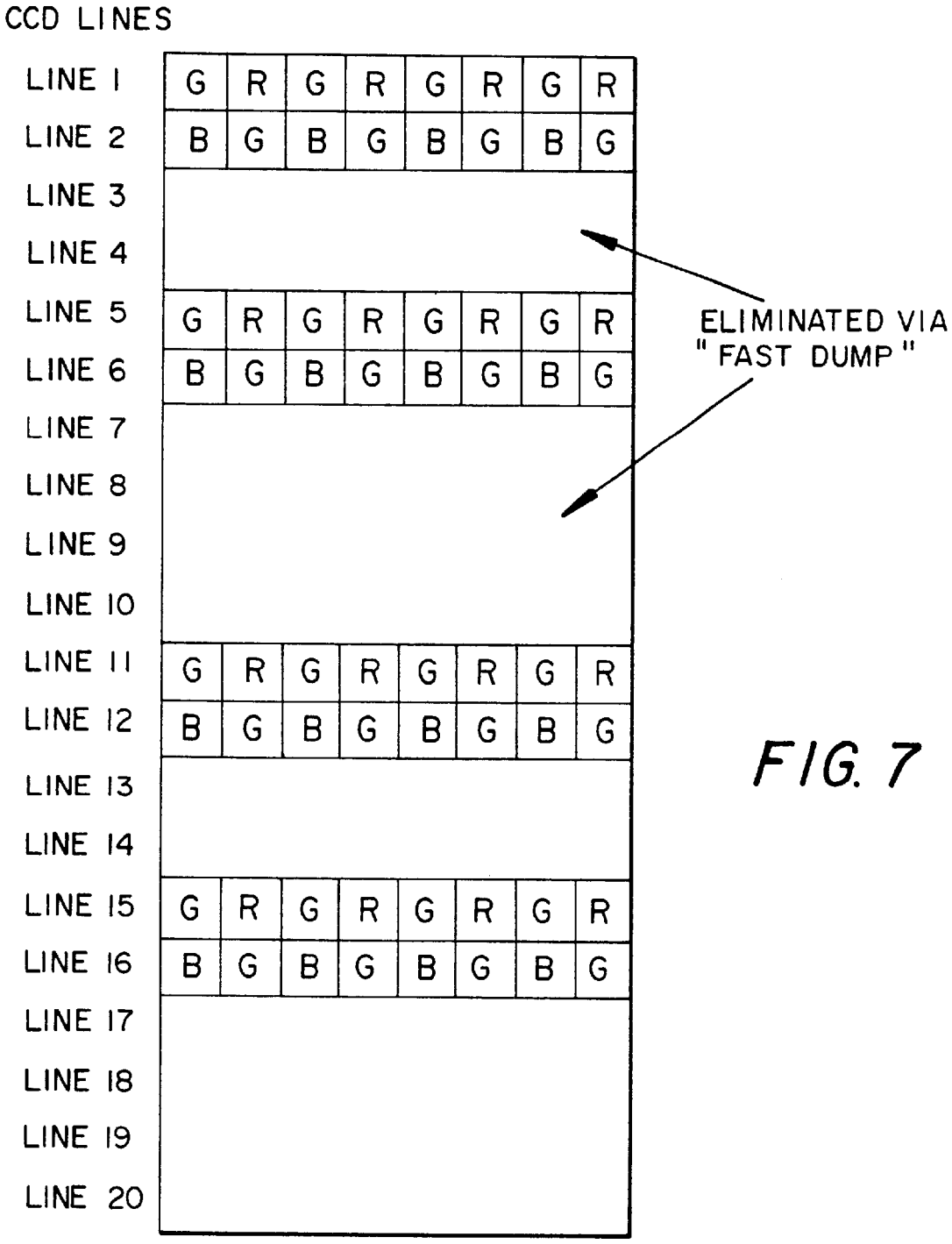

CCD LINES
LINE 1
LINE 2
LINE 3
LINE 4
LINE 5
LINE 6
LINE 7
LINE 8
LINE 9
LINE 10
LINE 11
LINE 12
LINE 13
LINE 14
LINE 15
LINE 16
LINE 17
LINE 18
LINE 19
LINE 20
G R G R G R G R
B G B G B G B G
ELIMINATED VIA
" FAST DUMP "

FIG. 7

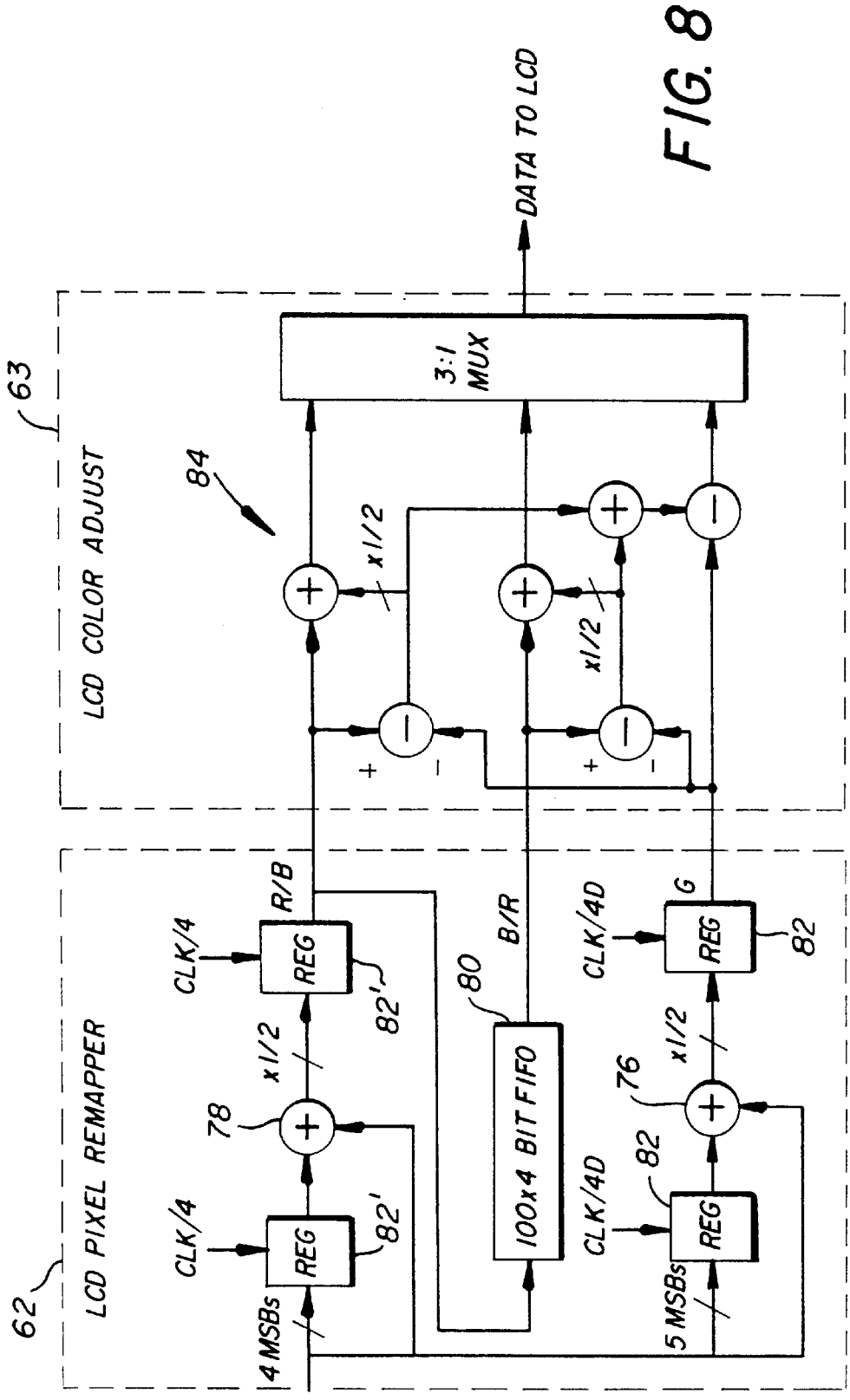

DATA TO LCD
63
LCD COLOR ADJUST
3:1 MUX
84
x1/2
x1/2
62
LCD PIXEL REMAPPER
CLK/4
R/B
REG
82'
x1/2
78
CLK/4
REG
82'
4 MSBs
80
B/R
100x4 BIT FIFO
CLK/4D
G
REG
82
x1/2
76
CLK/4D
82
REG
5 MSBs

FIG. 8

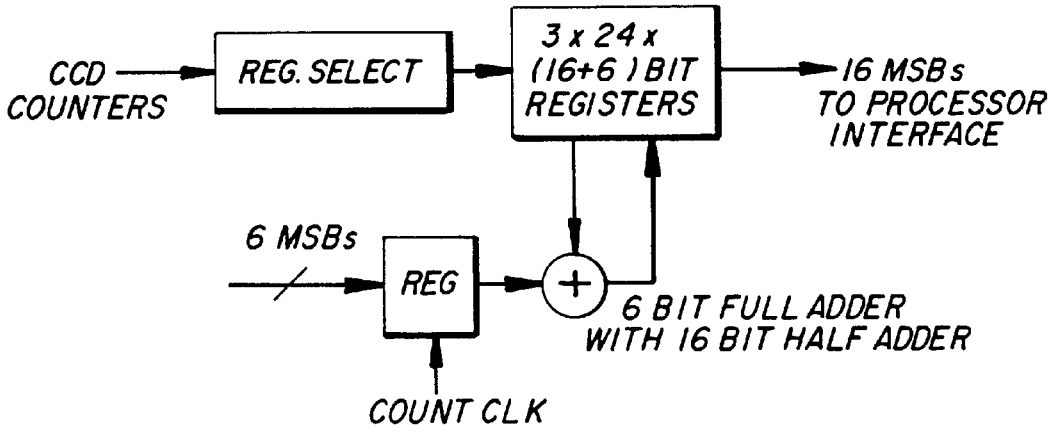

CCD COUNTERS
REG. SELECT
3 x 24 x (16+6) BIT REGISTERS
16 MSBs TO PROCESSOR INTERFACE
6 MSBs
REG
6 BIT FULL ADDER WITH 16 BIT HALF ADDER
COUNT CLK

FIG. 9A

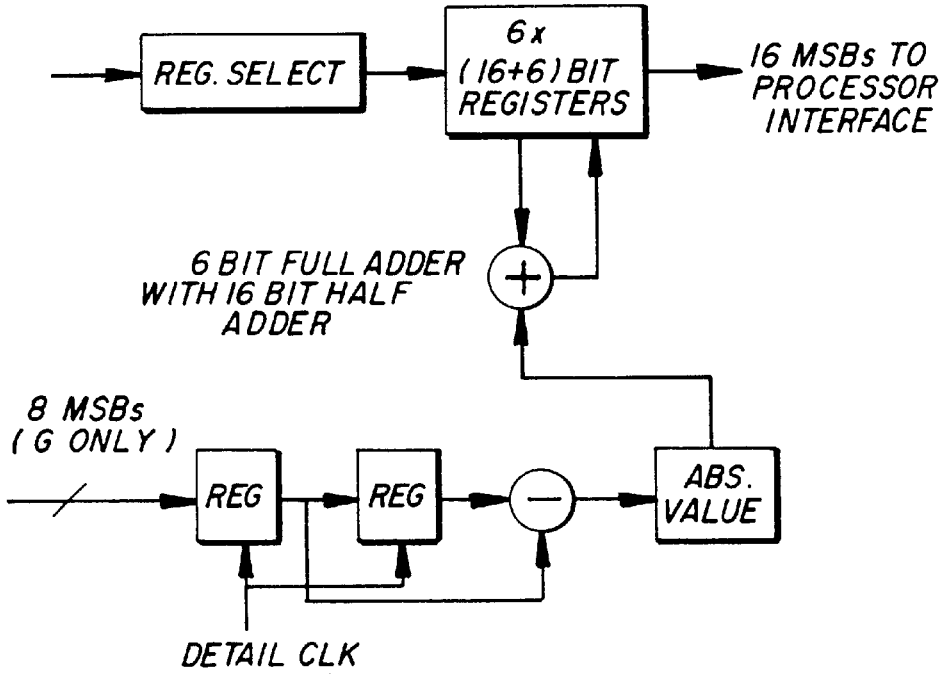

REG. SELECT
6 x (16+6) BIT REGISTERS
16 MSBs TO PROCESSOR INTERFACE
6 BIT FULL ADDER WITH 16 BIT HALF ADDER
8 MSBs (G ONLY)
REG
REG
ABS. VALUE
DETAIL CLK

FIG. 9B

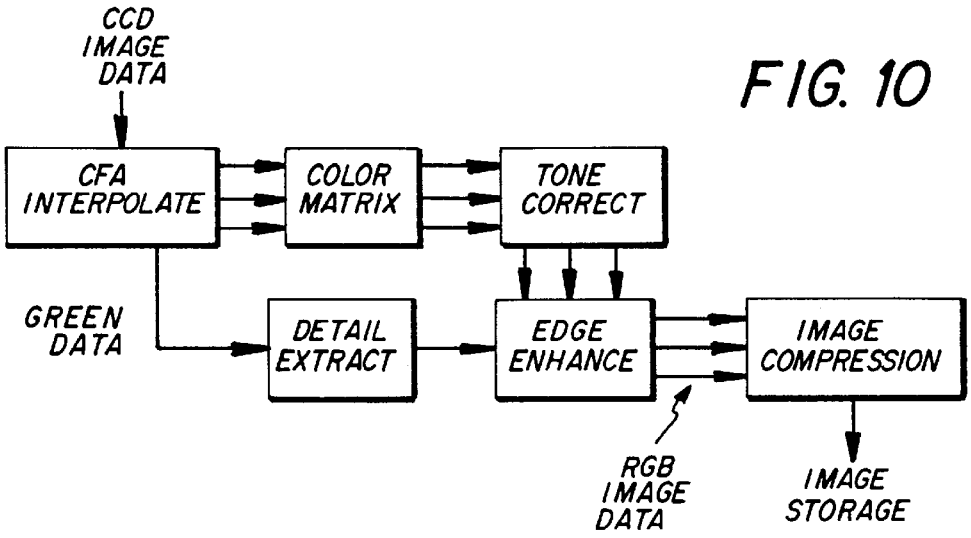



FIG. 10

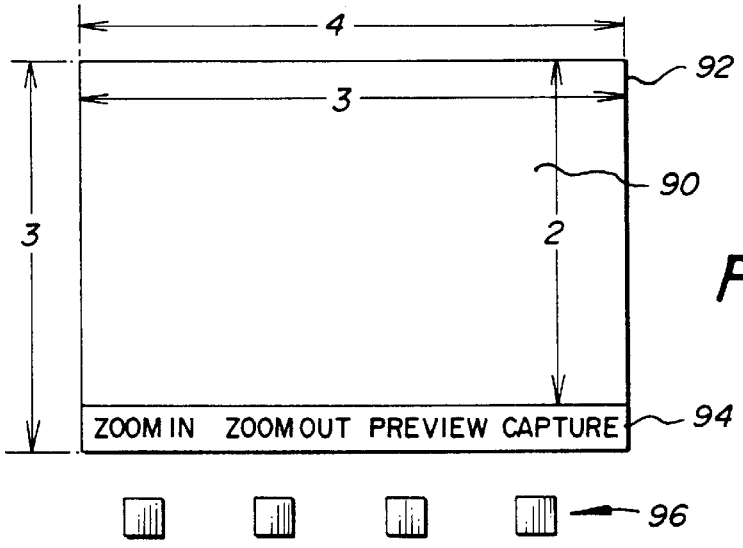



FIG. 11

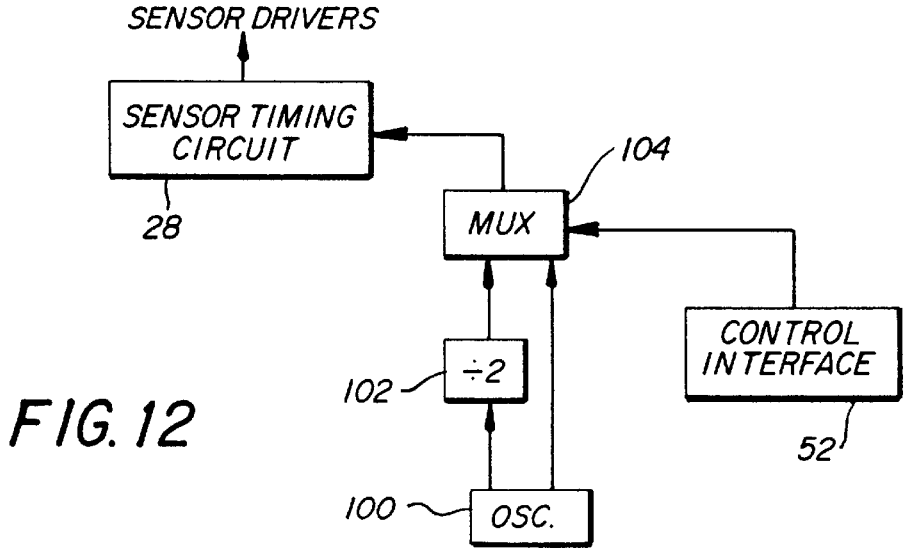



FIG. 12

# ELECTRONIC CAMERA FOR INITIATING CAPTURE OF STILL IMAGES WHILE PREVIEWING MOTION IMAGES

This application is a division of 08/367,399 filed Dec. 30, 1994.

## FIELD OF THE INVENTION

The invention pertains to an electronic still camera for composing and capturing still images, and, more particularly, to an electronic camera having a "motion" mode for previewing a scene and a "still" mode for capturing a particular image in the scene.

## BACKGROUND OF THE INVENTION

Consumer camcorders which include the capability of recording analog motion and/or still images on 8mm or VHS videotape have been developed by a number of companies. Motion images are recorded in the same manner as in any standard camcorder. These cameras include a single chip charge coupled device (CCD) sensor having a color filter array that provides a spatially color-sampled image. To record still images, the user pushes a "still capture" button at the desired instant. The image obtained from the CCD sensor is temporarily stored in a digital memory. The image is then read from the memory and recorded onto the videotape. Some camcorders include color liquid crystal displays (LCD), which are also spatially color-sampled devices. Some are relatively large, for example, ranging from approximately 2.5" to 4" in diagonal. Such a display is used, instead of a normal eyepiece viewfinder, to allow the user to properly frame the subject and view the images as they are being recorded. It is also used to view the recorded images as the videotape is played back.

FIG. **1**A shows a typical color LCD display, in which the liquid crystal material is trapped between an upper glass plate **1** and a lower glass plate **2**. The upper plate **1** has a common transparent electrode **3** and an array **4** of color filters surrounded by a black mask **5**. The lower plate **2** includes an array **6** of transparent pixel electrodes juxtaposed underneath the array **4** of color filters. Individual pixel electrodes are activated via thin film transistors (TFT) **7** that are controlled from a video signal on the source lines **8** and a scanning signal on the gate line **9**. The LCD display includes the usual polarizer layers (not shown) on the glass plates **1** and **2**, such that activation of selected transparent pixel electrodes allows light to pass through the corresponding color filters and reflect to the viewer, thereby creating a color image. A typical LCD display such as the Epson LB 2F-BC00, manufactured by Seiko-Epson Company, Japan, has about 240 lines of pixels and about 300 pixels per line, with an image aspect ratio of 4:3. Such an aspect ratio allows the entire area of the image obtained from the 4:3 aspect ratio NTSC format CCD sensor to be displayed on the LCD screen, so that the LCD screen composition will be the same as the image that is recorded by the camcorder NTSC format recorder, for later display on an NTSC format television display. Note that because the LCD has only 240 lines of pixels, the interlaced NTSC signal is displayed using a "repeat field" technique, where both the odd and even fields from the NTSC format sensor are displayed using the same lines of pixels on the LCD. This LCD, like most commercially available LCDS, has "rectangular" pixels, rather than square pixels, where the distance between pixels in the horizontal direction is for example ⅔ the distance in the vertical direction. The LCD pixels are overlaid with a diagonal RGB stripe pattern as shown in FIG. **1**B.



In camcorders, the processing for both the still images and the motion images is identical. Such processing is normally implemented by hardwired analog integrated circuits, although camcorders which use digital image processing integrated circuits have been produced. Such camcorders convert the signal from the CCD sensor into an NTSC composite or component format signal, which is provided to a video recording subsystem or a video output jack. The color LCD display includes circuitry to decode the NTSC composite or component signal back into spatially subsampled RGB signals to drive the individual RGB pixels on the LCD sensor.

In a system oriented toward still photography, and in particular a digital still system, it would be desirable to avoid the necessity of generating an NTSC format signal in order to reduce the complexity of the required circuitry. In a totally digital system, that is, both the recording and display channels are digital, it is further desirable to minimize incompatibility between the channels. The problem is to achieve these objective in an architecture that minimizes cost and complexity and maximizes user handling.

## SUMMARY OF THE INVENTION

This problem is solved according to the invention by a number of features. In one aspect, the electronic camera is operable in a still image mode according to a relatively more complex digital image processing technique to produce high quality still images, and in a motion preview mode according to a relatively more simple digital image processing technique to produce a preview image of acceptable quality prior to initiation of the still image mode. Such an architecture is particularly adapted to mapping an array of color image pixels from a sensor into an array of color display pixels on an LCD display comprising discrete LCD display pixels fewer in number than image sensor pixels. In that case, a relatively simple digital processing technique combines samecolored image pixel signals into a fewer number of intermediate pixels that correspond to the arrangement of the color display pixels.

The advantage of the invention is that the two modes can be tailored for a relatively low quality "motion" mode and a much higher quality "still" mode. The motion mode images from the CCD sensor are processed by a hardwired digital signal processing circuit that generates low resolution, spatially subsampled digital image data which can directly drive the relatively low resolution LCD display. This reduces the complexity and clock frequency of the required circuitry, compared to generating an NTSC format signal, as is normally done in the prior art. The still mode image from the CCD sensor is processed by a general purpose processor (CPU) which executes an image processing software program in order to produce a high quality digital still image.

## BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be described in relation to the drawings, whereon

FIGS. **1**A and **1**B show the structure and color filter pattern of a known color liquid crystal display (LCD);

FIG. **2** is a block diagram of an electronic camera incorporating dual modes for composing and capturing a still image according to the invention;

FIGS. **3**A and **3**B are diagrams of progressive scan image sensors useful with the camera of FIG. **2**;

FIG. **4** is a diagram of the Bayer color filter geometry for the sensor used with the camera of FIG. **1**;

FIG. **5** shows the line timing for the still mode of operation;

FIGS. **6**A and **6**B show the line timing for the preview mode of operation;

FIG. **7** shows the special line skipping pattern used in the preview mode;

FIG. **8** shows further detail of the preview mode processing circuit shown in FIG. **2**;

FIGS. **9**A and **9**B show further detail of the image statistics processor shown in FIG. **2**;

FIG. **10** shows one example of still mode image processing;

FIG. **11** shows the effect of pixel mapping from a sensor to an LCD display, each having different aspect ratios; and

FIG. **12** shows an enhancement to the block diagram of FIG. **2** in which a different sensor clock frequency is used in each of the dual modes.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

A block diagram of a camera incorporating dual modes of processing according to the invention is shown in FIG. **2**. The camera includes an electronic color display, for example, a color liquid crystal (LCD) display **10** of the type shown in FIG. **1**A, and a user control section **12** having a number of user control buttons, including zoom buttons **14**, a preview button **15** and a capture button **16**. To take a still picture, the user turns on the camera (using a power switch (not shown), which may be automatically enabled when the user depresses the zoom buttons **14** or the preview button **15**, or partially depresses the capture button **16**). The user composes the picture by depressing the "zoom in" or "zoom out" buttons **14**, and by adjusting the position of the camera, while observing the display image. When the user is satisfied with the composition on the color LCD display **10**, the user depresses the capture button **16**. The camera then captures a single still image, firing a flash **18** if necessary when the ambient illumination level is low. The still image is focused upon an image sensor **20** by a motor driven zoom lens **22**. The intensity of the image light upon the sensor **20** is regulated by a motor-driven, variable, mechanical aperture **24**, while exposure time is regulated electronically by appropriate clocking of the sensor **20**. The still image from the image sensor **20** is processed and digitally stored on a removable memory card **26**.

Control of the sensor is provided by a timing and control section **27**, which is an application specific integrated circuit (ASIC) with processing and timing functions, for both capture and preview operating modes. For instance, the timing and control section **27** includes a sensor timing circuit **28** for controlling the image sensor functions. The sensor timing circuit **28** provides the signals to enable sensor drivers **30**, which provide horizontal clocks (H1, H2), vertical clocks (V1, V2), as well as a signal FDG for activating a drain structure on the sensor **20**. The output of the image sensor **20** is amplified and processed in an analog gain and sampling (correlated double sampling (CDS)) circuit **32**, and converted to digital form in A/D converter stage **34**. The A/D output signal is provided to a processor section **35**, which includes a digital processor **36** for temporarily storing the still images in a DRAM memory **38**. The digital processor **36** then performs image processing on the still images, and finally stores the processed images on the removable memory card **26** via a memory card interface circuit **40**, which may use the PCMCIA 2.0 standard interface. An EPROM memory **42** is used to store the firmware which operates the processor **36**. The components of the processor **35** are interconnected through a data bus **43**, which also connects to the timing and control section **27** and to the card interface **40**.

The motor-driven zoom lens **22** includes a zoom motor **44**, a focus motor **46**, and an aperture motor **48** (all controlled by lens motor drivers **50**). The timing and control section **27** further includes a control interface **52** connected to the lens motor drivers **50** and to a flash control circuit **53** via a photosystem interface block **54**, which controls the operation of the zoom lens **22** and the flash **18**. The lens zoom position is controlled by the photosystem interface block **54** based on position input from the zoom control buttons **14** through a user status and control section **55**. The focusing, exposure control, and white balance is done automatically, as is typically the case in consumer camcorders. This is done by computing "image statistics" in an image statistics processor **60** in the real-time ASIC (timing and control section **27**) as preview images are continuously read out of the image sensor **20**. The computed values are then used by a program implemented in the digital processor **36**, which decides how to adjust the focus motor, aperture, analog gain control, and analog white balance controls via the control interface **52** and the photosystems interface **54** on the ASIC timing and control section **27**. Although the digital processor **36** and the control interface **52** are shown as being within two separate sections, in some implementations the same component could be used to perform both of these functions (as well as other of the recited functions). Sensor image data is passed to the processor section **35** through a high speed interface **56** in the timing and control section **27**. The sensor image data is also directed to the color LCD display **10** through a preview mode processing circuit **58**.

The timing and control section (ASIC) **27** is operable in two modes, a relatively low quality "motion" mode and a much higher quality "still" mode. In the motion mode, images from the sensor **20** are processed by the preview mode processing circuit **58**; in the still mode, images from the sensor **20** are processed in the processor **35**. The processor **35** is a software driven digital processing system that is slower than the ASIC **27**. The preview mode processing circuit **58** is a hardwired digital signal processing circuit (part of the ASIC **27**) that generates low resolution, spatially subsampled digital image data which can directly drive the relatively low resolution color LCD display **10**. This reduces the complexity and clock frequency of the required circuitry, compared to generating an NTSC format signal, as is normally done in the prior art. The preview mode processing circuit includes a pixel remapper **62** for mapping the greater number of image pixels from the sensor **20** into the lesser number of display pixels (i.e., corresponding to the array **6** of transparent pixel electrodes in FIG. **1**) in the color LCD display **10**. The color saturation of the remapped pixels is then adjusted in a color adjustment circuit **63** and its output is applied to a multiplexer **64**. The multiplexer **64** selects image data either from the preview mode processing circuit **58**, producing a preview image, or from the high speed interface **56**, which allows for suitably preprocessed viewing of stored images.

In this camera, the image processing used to create the preview mode is done in the timing and control ASIC **27**, since the processing must be done rapidly. About **60** images per second are processed in preview mode. However, since the image quality of the displayed image is limited by the resolution and color gamut of the LCD screen of the LCD color display **10**, there is no need for elaborate image

processing. Therefore, simple "preview mode" image processing is performed in a fixed digital circuit embedded in the preview mode processing circuit **58** (which is part of the ASIC). The quality requirements for the still mode are much greater, since these images will be downloaded to a computer, and may be displayed on a high resolution CRT display, or printed on a high quality thermal printer. Therefore, the digital image processing must be more elaborate. By using the digital processor **36** to implement software procedures stored in the firmware memory **42**, complex procedures can be implemented. These procedures can take several seconds to complete, since real-time operation is not required. Use of firmware-stored software allows the still mode image processing to be upgraded without requiring a new ASIC design. In effect, what happens is that a relatively less complex digital image processing technique is used in the motion preview mode, but at a higher data rate, and a relatively more complex digital image processing technique is used in the still mode, but at a slower data rate.

Since the update rate, that is, the number of images that need to be supplied per unit time, is different for the still mode than for the motion mode, it is beneficial to use different clock frequencies for the different modes of operation. For example, as shown in FIG. **12**, a system oscillator **100** produces a 12 mHz clock frequency for use in the motion mode to obtain more updates/second (e.g., 60 images per second), while a divider **102** divides by two to provide a 6 mHz clock frequency for the still mode. The lower frequency allows more time to accurately position the clamp and sample pulses so as to avoid CCD output signal transitions. This increases noise immunity in the still mode. A multiplexer **104** is enabled by the control interface **52** to determine which clock frequency is applied to the sensor timing circuit **28**. Though not specifically shown, the changed timing is also communicated to the A/D stage **34** and other timing and control circuits.

The sensor **20** is a progressive scan interline image sensor having a noninterlaced architecture, as shown in more detail in FIG. **3**A. The sensor comprises a two-dimensional array of photosites **66**, e.g. photodiodes, arranged in rows and columns of image pixels, a plurality of vertical registers **68** adjacent photosite columns for transferring rows of image pixel charge from the photosites **66** to a horizontal register **70** for readout responsive to clock signals from the sensor drivers **30**, and a charge drain (specifically, a fast dump structure **72**) interposed between the output of the vertical registers **68** and the horizontal register **70** for eliminating complete rows of image pixels at a time from the image sensor **20**. A preferred image sensor is the Kodak model CCD KAI-0400CM image sensor, which has approximately 512 active lines with approximately 768 active pixels per line and an image aspect ratio of 3:2. This sensor is described in a Performance Specification document available from Eastman Kodak Company, Rochester, N.Y. Each pixel is 9 microns "square", since both the vertical and horizontal distances between the centers of adjacent pixels are 9 microns. The 3:2 image aspect ratio of the CCD sensor, although wider than the 4:3 aspect ratio of the display, is considered to be a preferred aspect ratio for still photography, in that the standard 35 mm film format, and standard 4R (4"×6") prints also have a 3:2 image aspect ratio. The sensor uses a color filter array pattern known as the "Bayer checkerboard" pattern, described in U.S. Pat. No. 3,971,065, which is shown in FIG. **4**. Such a color filter array is characterized by a mosaic pattern in which the filter colors alternate in both line and column directions. In the normal operating mode, all of the image pixels on the sensor are transferred as color image pixels to the horizontal register **70**, which delivers a stream of color pixel signals to the analog gain and CDS circuit **32** (see FIG. **2**). The color pixel signals are subsequently converted to digital pixel signals in the A/D converter **34**.

The sensor **20** uses a progressive scan readout method, which allows the entire image to be read out in a single scan. The accumulated or integrated charge for the photodiodes comprising the pixels **66** is transported from the photosites to light protected vertical (parallel) registers **68** by applying a large positive voltage to the phase-one vertical clock (**V1**). This reads out every row, or line, into the vertical registers **68**. The image pixel charge is then transported from the vertical registers **68** to the horizontal register **70** by two-phase clocking of the vertical clocks (**V1**, **V2**). Between the vertical and horizontal registers is the fast dump structure **72**, which is further described in the Performance Specification document for the KAI-0400CM sensor. By setting a suitable positive potential on a fast dump gate line FDG, charge from the row of pixel values currently adjacent to the fast dump structure **72** is transferred from the CCD directly into the sensor substrate **74** rather than to the horizontal register **70**. This dump, or line clear, is accomplished during the vertical-to-horizontal transfer time. When properly controlled by the sensor timing circuit **28**, the fast dump structure **72** allows lines of charge to be eliminated.

The timing and control section **27** operates the electronic camera shown in FIG. **2** in the two aforementioned modes, including a first "still" mode wherein all rows of image pixel charge corresponding to each line are progressively read out through the horizontal register **70** during a single scan, and a second "motion" mode wherein some of the rows of image pixel charge corresponding to some lines are eliminated through the fast dump structure **72** prior to readout. As applied to the embodiment of FIG. **2**, the first mode corresponds to a high quality still imaging mode while the second mode corresponds to a special "line skipping" mode for driving the color LCD display **10**. In the second mode, the timing and control section **27** controls the fast dump structure **72** to eliminate two or more consecutive lines of image charge from the image sensor **20** for every one or more lines of image charge that are transferred to the horizontal register **70** for readout, thereby generating a pattern of lines (shown in FIG. **7**) suitable for driving the LCD display in a "repeat field" mode. An appropriate video signal which displays the entire 3:2 aspect ratio sensor image on the 4:3 aspect ratio LCD, without introducing geometric distortion, is generated by alternately eliminating two or four consecutive lines of image charge for every pair of lines of image charge that are transferred to the horizontal register **70**.

The sensor timing circuit **28** is controlled by the control interface **52** to provide the clock signals **V1**, **V2**, **H1**, **H2**, and the gate signal FDG according to the two modes of operation. The timing signals for the first mode are shown in FIG. **5**; those for the second mode are shown in FIGS. **6***a* and **6***b*. The two-phase cycling of signals **V1** and **V2** control the transfer of lines of image pixel charge from the vertical registers **68** to the horizontal register **70**. The two-phase cycling of signals **H1** and **H2** control the transfer of a stream of color pixel signals from the horizontal register **70** to subsequent circuits in the camera. The level of the signal FDG determines whether the image charge is dumped to the substrate **74** or transferred to the horizontal register **70**. When the sensor **20** is clocked using the first timing mode shown in FIG. **5** for all lines of the sensor, all lines of the sensor are clocked out, one after the other, through the horizontal register **70**, processed in subsequent camera

circuitry, and stored in the removable memory **26**. This timing mode provides a high quality progressive scan still image, but may take 1/30 second or longer to read out the still image. Such timing, however, is acceptable for still mode usage, and, as mentioned before, does not require unusually high speed components and, indeed, may benefit from a lower speed lock.

To provide an image to the color LCD display **10**, a lower resolution image is suitable, but the update rate must be sufficient to provide good motion rendition and eliminate display flicker. Moreover, the sensor **20** includes the aforementioned array of color filters arranged in a particular mosaic color pattern (e.g., the checkerboard Bayer pattern of FIG. **3**), and the lines of image charge that are transferred to the horizontal register **70** should preserve that particular color pattern in the pattern of lines that are generated for the line-skipping readout. To provide this kind of image, the sensor is read out in the second mode as shown in FIG. **7**, using the timing shown in FIGS. **6**A and **6**B. As shown in FIG. **6**A, the first two lines (**1** and **2**) are read out as in the normal mode. These provide a green-red and a blue-green line. The next two lines (**3** and **4**) are eliminated by turning on the fast dump structure **72** during the time that these lines are transferred past the fast dump structure **72**. Next, as shown in FIG. **6**B, lines **5** and **6** are read out normally, and then lines **7**, **8**, **9**, and **10** are eliminated. Next, the FIG. **6**A timing is used to read out lines **11** and **12**, while eliminating lines **13** and **14**, and then the FIG. **6**B timing is used to read out lines **15** and **16**, while eliminating lines **17**–**20**. This process proceeds for the entire image readout period, during which **102** pairs of lines are read out, and 154 pairs of lines are eliminated.

This special "line skipping" readout mode, as shown in FIG. **7**, allows the sensor 3:2 aspect ratio image to be fully displayed on a 4:3 aspect ratio LCD without "geometric distortion", that is, without stretching the image vertically, and without cropping off the horizontal edges of the image from the image sensor. This allows the LCD to properly show the entire 3:2 aspect ratio image captured by the sensor, so that an image can be properly composed.

As the 512 lines of the CCD imager are read out using the special "line skipping" mode, they are displayed using only 204 out of the approximately 240 LCD lines of pixels. The remaining approximately 36 lines can either be masked behind a bezel, so that they are not visible, or preferably may be used to display status information, such as the time-of-day, image number, or a "push-button menu" for the user buttons. FIG. **11** shows a useful application of such conversions. A sensor having a 3:2 aspect ratio is shown mapped into an image area **90** of an LCD display screen **92** having a 4:3 aspect ratio. A proportional remapping leaves a status area **94** available for other purposes, specifically to show text indicating the function of a set of reconfigurable control buttons **96** in the control section **12**. The function of the buttons is specified by the user status and control section **55** (FIG. **2**). This status information graphics data can be supplied by the digital processor to the LCD **10** via high speed interface **56**, when the MUX **64** is controlled so as to use the digital data from interface **56**, rather than from circuit **58**, for supplying data to the final approximately **32** lines of the display **10**.

The "line skipping" readout causes some minor vertical sampling artifacts, but these are not noticeable in the small LCD displays. The pixels output for the sensor **20** in line skipping mode continue to have the Bayer-type color filter repeating pattern, so that they can be processed using processing techniques designed for the Bayer pattern.

The processing complexity of the camera of FIG. **2** is considerably simplified by directly mapping the RGB sensor pixels **66** to the RGB pixels of the display **10**. The easiest way to do this for the image sensor **20** (512 lines×768 pixels and 3:2 aspect ratio) is to have an LCD display with 512×768 pixels and the same aspect ratio and color filter pattern. However, this would be a custom, costly LCD. Instead, LCDs have fewer display pixels than image pixels on the image sensor, normally have a 4:3 image aspect ratio, and use the diagonally striped RGB pattern shown in FIG. **1**B. In this discussion, an LCD pixel array of about 240 lines×312 pixels per line is assumed.

Therefore, the sensor pixels are processed in a "pixel mapping circuit", such as the LCD pixel remapper **62**. A block diagram of this circuit is shown in FIG. **8**. Note that there are 768/2=384 green or red/blue pixels per line on the sensor (see FIG. **4**). There are about 300/3=100 green, red, or blue pixels per line on the LCD (see FIG. **1**B). Thus, there are approximately ¼ as many LCD pixels per line (per color) as there are sensor pixels per line. Therefore, the basic plan is to combine same-colored image pixels into a fewer number of intermediate, combination pixel signals that are then mapped into the color display pixels. For instance, a simple "pixel mapping" circuit maps four green sensor pixel signals into one green LCD pixel for one line by summing two green sensor values, spaced apart by 4 CCD pixel positions, in the green pixel summer **76** and dividing by two via bit-shift wiring. The necessary delay is provided by the registers **82** clocked at one fourth the pixel rate, further delayed by one pixel clock. It also maps four red sensor pixels into one LCD pixel in the same manner (using the red/blue summer **78**), and also stores this value in a 100 pixel FIFO **80**. The FIFO **80** compensates for the fact that the sensor has line sequential red and blue pixels, by supplying blue pixels on the red sensor lines, and red pixels on the blue sensor lines. Four pixel delays are provided by the registers **82'** clocked at one fourth pixel rate (CLK/4). The mapping process is basically, therefore, a process which, in its simplest form, involves averaging of signals to produce a smaller number of output color pixels than input color pixels. (The CFA interpolation algorithm discussed in reference to FIG. **10**, on the other hand, produces a larger number of "output" color pixels than input color pixels.) Alternate groups of 2 or 4 lines of sensor values are discarded during preview mode by using the fast dump gate shown in FIG. **3**A, as described in connection with the "line skipping" mode. This allows the sensor readout time to be decreased by more than ½ during the preview mode.

Another feature of the design is that by removing the NTSC rate driving circuitry from the color LCD display **10**, the active matrix LCD can be updated at a slower frequency than is normally used. This reduces the cost and power consumption of the LCD driver circuits (not shown). For example, the LCD can be updated at 30 Hz (provided the LCD active matrix display is designed so as not to exhibit noticeable flicker at this update rate), instead of 60 Hz.

Once the LCD pixel values are calculated, the LCD color adjust circuit **63** increases the color saturation of the image by forming R-G and B-G color difference signals, and adding or subtracting a fraction of these signals in an array **84** of adders and subtractors from the original RGB signals in order to increase the color saturation of the displayed image. This circuit performs a similar function as a 3×3 color matrix, but uses less hardware and provides less color accuracy. The color accuracy is not critical for the LCD display, however, due to the limited color reproduction quality of such displays. The color reproduction of the still

image is much more important, and is done with a more complicated and precise color correction method with the stored firmware in EPROM **42**.

FIGS. **9**A and **9**B show the processing in the image statistics processor **60**, which computes real-time values for both still and motion image capture, all during the preview mode. These values include 24 R, G, and B averages used to set white balance and exposure, and 6 average high frequency "detail" values used to set focus. The 24 RGB averages for white balance are calculated for a group of 4×6 rectangular image regions, for each of R, G, and B; a block diagram of the calculation in one color is shown in FIG. **9**A. The 6 average "detail" values for focusing are calculated for green pixels only by accumulating the absolute value of the differences between nearby green values; a block diagram of this calculation is shown in FIG. **9**B. These values are computed for each preview image and downloaded to the processor **36**. The processor **36** implements a firmware stored procedure which determines the optimum exposure parameters (exposure time, f/stop, and analog gain), white balance settings, and lens focus setting. For the still mode, the processor **36** also decides, based on the last preview images, whether to fire the flash, and determines the optimum exposure parameters, white balance settings, and lens focus setting for the still mode.

Once the still image is captured, the digital processor **36** implements the stored firmware procedures to process and store the still image. FIG. **10** shows a diagram of one possible still image processing method. The CFA interpolation diagram may include the green interpolation method described in U.S. patent application Ser. No. 085,520, filed Jun. 30, 1993, in the name of the same assignee as the present application, and the chrominance interpolation method described in U.S. Pat. No. 4,642,678, both of which are incorporated herein by reference. The color matrix, tone correction, and edge enhancement steps may be similar to those described in U.S. Pat. No. 5,189,511, also incorporated herein by reference. The image compression method may be the JPEG standard compression technique.

The foregoing description envisions taking a single still picture following the motion preview mode. The camera can also optionally capture "bursts" of high quality still images into the DRAM memory during the "still" mode, which are then processed as shown in FIG. **10**. Owing to the flash recharge time and other limitations of the "burst" mode, the "burst" mode could utilize different exposure parameters (exposure time, aperture, analog gain, flash, and digital processing) than either the motion or the single still mode.

The invention has been described with reference to a preferred embodiment. However, it will be appreciated that variations and modifications can be effected by a person of ordinary skill in the art without departing from the scope of the invention. For instance, FIG. **3**B shows a progressive scan sensor with two readout registers **86** and **88** (which corresponds to the Performance Specification document for the Kodak KAI-031CM image sensor; the preferred embodiment of FIG. **3**A simply uses but one register). The purpose is to eliminate the FIFO line delay **80** in the LCD pixel remapper **62**. The pairs of lines read out by the registers include both a green/red line and a blue/green line. Therefore, by adding an analog multiplexer between the outputs of the two channels and the analog gain and CDS block **32**, which is switched at ½ the sensor horizontal clock rate, it is possible to obtain a GRBG sequence of sensor data values at the output of the A/D stage **34**. The LCD pixel remapper **62** can then be designed to map from the CCD sensor color pixel pattern to the required RGBRGB LCD pixel pattern, without using a line delay. Since two CCD lines are read out in parallel, for each LCD line, fewer lines are eliminated via the fast dump gate than for the single-register sensor shown in FIG. **3**A.

In particular, if the dual register CCD in FIG. **3**B had 512×768 square pixels with a 3:2 aspect ratio, and the LCD had approximately 240 display lines and a 4:3 aspect ratio, the CCD readout would involve fast dumping one pair of lines for every four pairs of lines read out from the CCD sensor. The pixel readout procedure for the horizontal registers can then be varied depending on the mode of operation: both registers are used for the motion imaging mode and one register is used for the still imaging mode. Furthermore, although the Bayer pattern was described, other mosaic-type filter patterns could be used to advantage, for example, complementary patterns involving cyan, magenta, yellow and green filters. The processing for the LCD pixel remapper **62** and the LCD color adjust circuit **63** would be accordingly modified to account for the different color arrangement.

PARTS LIST

**1** upper plate
**2** lower plate
**3** common transparent electrode
**4** array of color filters
**5** black mask
**6** array of transparent pixel electrodes
**7** thin film transistors
**8** source lines
**9** gate line
**10** color LCD display
**12** control section
**14** zoom buttons
**15** preview button
**16** capture button
**18** flash
**20** progressive scan interline
**22** zoom lens
**24** mechanical aperture
**26** memory card
**27** timing and control section
**28** sensor timing circuit
**30** sensor drivers
**32** analog gain and CDS
**34** A/D converter
**36** digital image processor
**38** DRAM memory
**40** card interface
**42** EPROM memory
**44** zoom motor
**46** focus motor
**48** variable aperture
**50** lens motor drivers
**52** control interface
**53** flash control circuit
**54** photosystems interface
**55** user status and control section
**56** high speed interface
**58** preview mode processing circuit
**60** image statistics processor
**62** pixel remapper
**63** color adjustment circuit
**64** multiplexer
**66** pixel
**68** vertical readout register
**70** horizontal register

**72** fast dump structure
**74** sensor substrate
**76** green pixel summer
**78** red/blue summer
**80** fifo
**82** two pixel delay registers
**84** array
**86** first readout register
**88** second readout register
**90** image area
**92** LCD display screen
**94** status area
**96** reconfigurable buttons
**100** oscillator
**102** divider
**104** multiplexer

What is claimed is:

**1**. An electronic still camera for initiating capture of a still image while previewing motion images on a display, comprising:

(a) an image sensor having a two-dimensional array of photosites covered by a mosaic pattern of color filters including at least three different colors for capturing images of a scene, each captured image having a first number of color pixel values provided in a first color pattern;

(b) motion processing means for generating from the captured images, a second number of color pixel values provided in a second color pattern having at least three different colors and representative of a series of motion images to be previewed, the second number of color pixel values being less than the first number of color pixel values, and the second color pattern being different from the first color pattern;

(c) a color display for presenting at least some of the motion images of the series of motion images corresponding to the captured images of the scene, the color display having an arrangement of color display pixels including at least three different colors in a pattern different from the first color pattern;

(d) a capture button for initiating capture of a still image while previewing the motion images presented on the color display;

(e) still processing means for generating a third number of color pixel values including at least three different colors representative of a processed captured still image; and

(f) a digital memory for storing the processed captured still image.

**2**. The electronic still camera of claim **1** further including a multiplexer having first and second inputs and an output, wherein the first input is coupled to the first processing means, the second input is coupled to the second processing means, and the output is coupled to the display so that a captured still image can be viewed on the display.

**3**. The electronic still camera of claim **1** wherein the first processing means and the second processing means are integrated into a single integrated circuit.

**4**. The electronic still camera of claim **1** wherein the motion processing means and the still processing means produce the second number of pixels and the third number of pixels, respectively, prior to transferring the image pixels to the display and the digital memory, respectively.

**5**. The electronic still camera of claim **1** wherein the second number of pixel values representative of the series of motion images are transferred to the display in a digital format.

**6**. The electronic still camera of claim **1** wherein the second number of pixel values representative of the series of motion images are mapped into a form suitable for display.

**7**. The electronic still camera of claim **6** wherein after the second number of pixel values representative of the series of motion images are mapped into a form suitable for display, the signals representing the captured images are converted back into an analog form.

**8**. The electronic still camera of claim **1** further including a firmware memory, a processor, and an application specific integrated circuit, and wherein the first processing means is provided in the application specific integrated circuit, and the second processing means is provided using the processor which implements software procedures stored in the firmware memory.

**9**. The electronic still camera of claim **1** wherein the image sensor includes a color filter array to produce color image data, the second processing means processes the color image data and performs JPEG image compression on the captured still image, and the JPEG compressed still image is stored in the digital memory.

**10**. The electronic still camera of claim **9** wherein the digital memory is a removable memory card.

**11**. The electronic still camera of claim **1** wherein the first color pattern includes substantially one-half green color filters.

**12**. The electronic still camera of claim **11** wherein the color display pixels are arranged in a pattern having substantially one-third green color filters.

**13**. The electronic still camera of claim **1** wherein the first color pattern is a Bayer checkerboard pattern.

**14**. The electronic still camera of claim **1** wherein the distance between adjacent image sensor photosites in the horizontal direction are substantially equal to the distance between the adjacent image sensor photosites in the vertical direction, and wherein the distance between the adjacent color display pixels in the horizontal direction is different than the distance between the adjacent color display pixels in the vertical direction.

**15**. An electronic still camera for initiating capture of a still image while previewing motion images on a display, comprising:

(a) an image sensor having a two-dimensional array of photosites covered by a mosaic pattern of color filters including at least three different colors for capturing images of a scene, each captured image having a first number of color pixel values provided in a first color pattern;

(b) a motion processor for generating from the captured images, a second number of color pixel values provided in a second color pattern having at least three different colors and representative of a series of motion images to be previewed, the second number of color pixel values being less than the first number of color pixel values, and the second color pattern being different from the first color pattern;

(c) a color display for presenting at least some of the motion images of the series of motion images corresponding to the captured images of the scene, the color display having an arrangement of color display pixels including at least three different colors in a pattern different from the first color pattern;

(d) a capture button for initiating capture of a still image while previewing the motion images presented on the color display;

(e) a still processor for generating a third number of color pixel values including at least three different colors representative of a captured still image; and

(f) a digital memory for storing the processed captured still image.

**16**. The electronic still camera of claim **15** further including a multiplexer having first and second inputs and an output, wherein the first input is coupled to the first processor, the second input is coupled to the second processor, and the output is coupled to the display so that a captured still image can be viewed on the display.

**17**. The electronic still camera of claim **15** wherein the first processor and the second processor are integrated into a single integrated circuit.

**18**. The electronic still camera of claim **15** wherein the motion processor and the still processor produce the second number of pixels and the third number of pixels, respectively, prior to transferring the image pixels to the display and the digital memory, respectively.

**19**. The electronic still camera of claim **15** wherein the second number of pixel values representative of the series of motion images are transferred to the display in a digital format.

**20**. The electronic still camera of claim **15** wherein the second number of pixel values representative of the series of motion images are mapped into a form suitable for display.

**21**. The electronic still camera of claim **20** wherein after the second number of pixel values representative of the series of motion images are mapped into a form suitable for display, the signals representing the captured images are converted back into an analog form.

**22**. The electronic still camera of claim **15** further including a firmware memory, and an application specific integrated circuit, and wherein the first processor is provided in the application specific integrated circuit, and the second processor implements software procedures stored in the firmware memory.

**23**. The electronic still camera of claim **15** wherein the image sensor includes a color filter array to produce color image data, the second processor processes the color image data and performs JPEG image compression on the captured still image, and the JPEG compressed still image is stored in the digital memory.

**24**. The electronic still camera of claim **23** wherein the digital memory is a removable memory card.

**25**. The electronic still camera of claim **15** wherein the first color pattern includes substantially one-half green color filters.

**26**. The electronic still camera of claim **25** wherein the color display pixels are arranged in a pattern having substantially one-third green color filters.

**27**. The electronic still camera of claim **15** wherein the first color pattern is a Bayer checkerboard pattern.

**28**. The electronic still camera of claim **15** wherein the distance between adjacent image sensor photosites in the horizontal direction are substantially equal to the distance between the adjacent image sensor photosites in the vertical direction, and wherein the distance between the adjacent color display pixels in the horizontal direction is different than the distance between the adjacent color display pixels in the vertical direction.

* * * * *

# EXHIBIT B: U.S. PATENT 5,493,335

US005493335A

# United States Patent [19]

**Parulski et al.**

[11] **Patent Number: 5,493,335**

[45] **Date of Patent: Feb. 20, 1996**

[54] **SINGLE SENSOR COLOR CAMERA WITH USER SELECTABLE IMAGE RECORD SIZE**

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[73] Assignee: **Eastman Kodak Company**, Rochester, N.Y.

[21] Appl. No.: **85,516**

[22] Filed: **Jun. 30, 1993**

[51] **Int. Cl.**[6] ..... **H04N 5/76**

[52] **U.S. Cl.** ..... **348/233**; 348/273; 358/906; 358/909.1

[58] **Field of Search** ..... 358/209, 909, 358/906, 909.1; 348/207, 266, 272, 273, 233; H04N 5/30, 5/76

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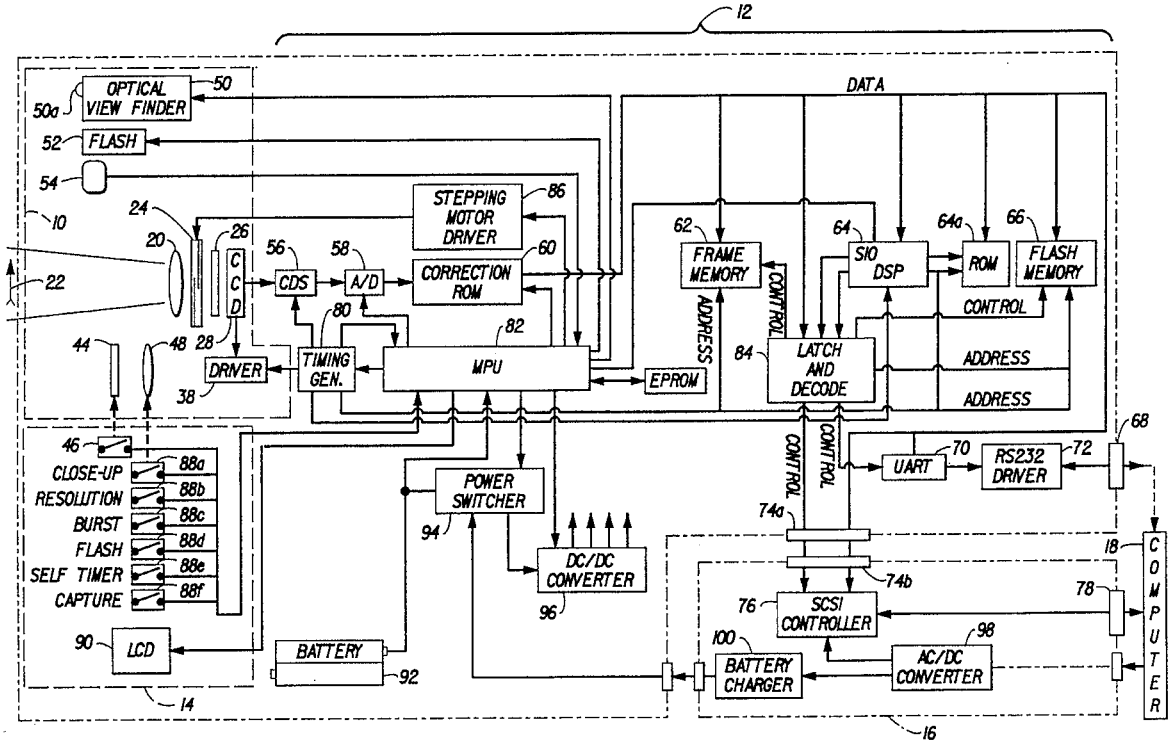
*Primary Examiner*—James J. Groody
*Assistant Examiner*—Cheryl Cohen
*Attorney, Agent, or Firm*—David M. Woods

[57] **ABSTRACT**

An electronic camera is adapted for processing images of different resolution to provide a user selectable image record size. A buffer memory is provided for storing color image pixels from a sensor as baseband signals corresponding to at least one image. A timing controller responsive to a resolution mode switch controls the order in which color image pixels are selected for storage in both vertical and horizontal directions. The order selected by the resolution switch includes a full resolution mode, and at least one reduced resolution mode in which the color image pixels are subsampled such that each chrominance image pixel is selected to be spatially adjacent to a selected luminance image pixel. Additionally, the buffer memory can store a burst of low resolution images.

**15 Claims, 5 Drawing Sheets**



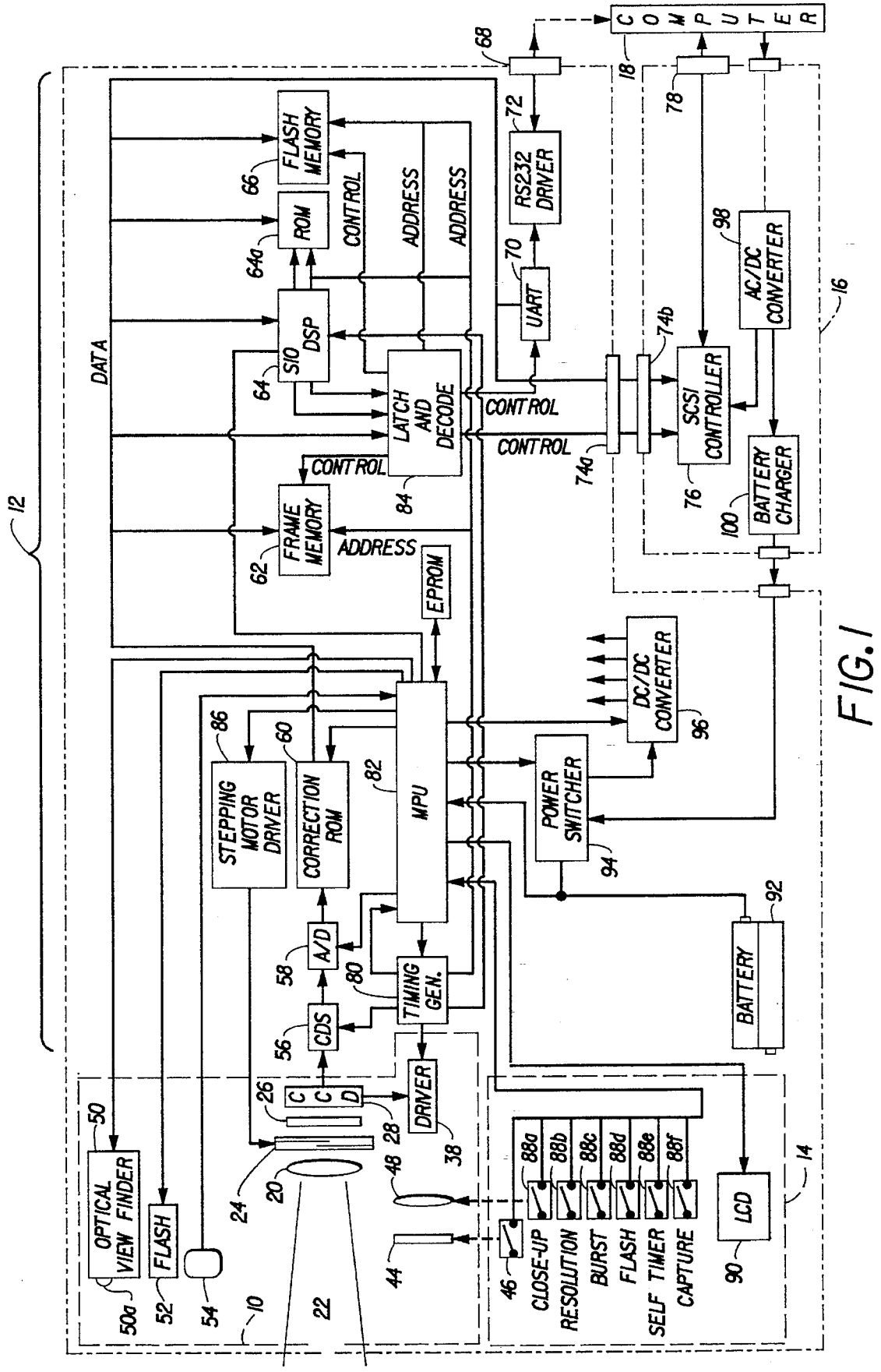

COMPUTER
18
68
78
72
RS232 DRIVER
70
UART
FLASH MEMORY
66
ROM
64a
SIO DSP
64
DATA
ADDRESS
ADDRESS
CONTROL
LATCH AND DECODE
84
CONTROL
CONTROL
74a
74b
SCSI CONTROLLER
76
98
AC/DC CONVERTER
16
BATTERY CHARGER
100
12
FRAME MEMORY
62
ADDRESS
EPROM
DC/DC CONVERTER
96
86
STEPPING MOTOR DRIVER
60
CORRECTION ROM
82
MPU
POWER SWITCHER
94
92
BATTERY
A/D
58
80
TIMING GEN.
CDS
56
26
C
C
D
DRIVER
28
38
48
50
OPTICAL VIEW FINDER
FLASH
24
20
44
50a
52
54
10
22
46
88a
88b
88c
88d
88e
88f
CLOSE-UP
RESOLUTION
BURST
FLASH
SELF TIMER
CAPTURE
LCD
90
14

FIG. 1

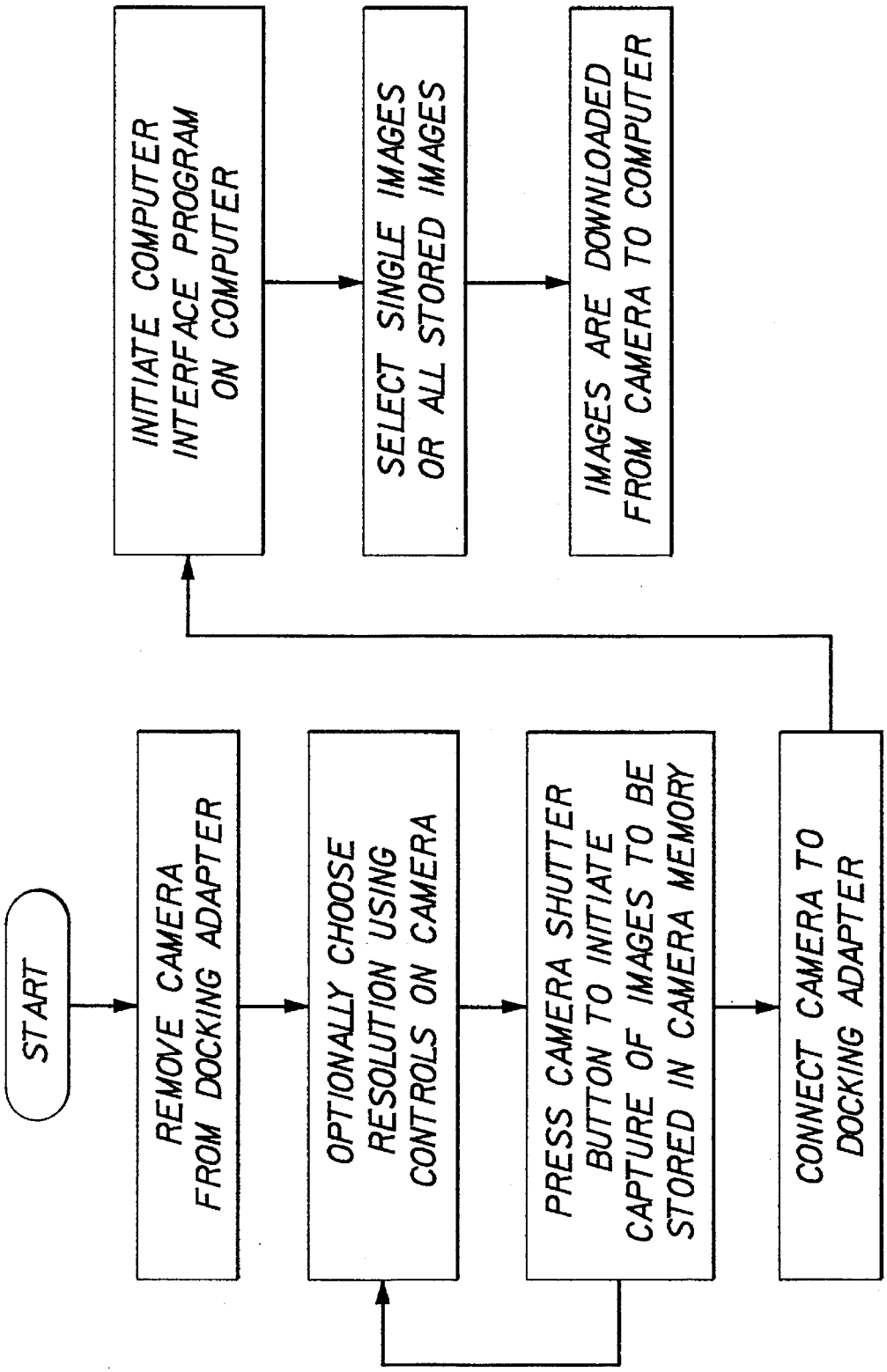

START
REMOVE CAMERA FROM DOCKING ADAPTER
OPTIONALLY CHOOSE RESOLUTION USING CONTROLS ON CAMERA
PRESS CAMERA SHUTTER BUTTON TO INITIATE CAPTURE OF IMAGES TO BE STORED IN CAMERA MEMORY
CONNECT CAMERA TO DOCKING ADAPTER
INITIATE COMPUTER INTERFACE PROGRAM ON COMPUTER
SELECT SINGLE IMAGES OR ALL STORED IMAGES
IMAGES ARE DOWNLOADED FROM CAMERA TO COMPUTER

FIG. 2

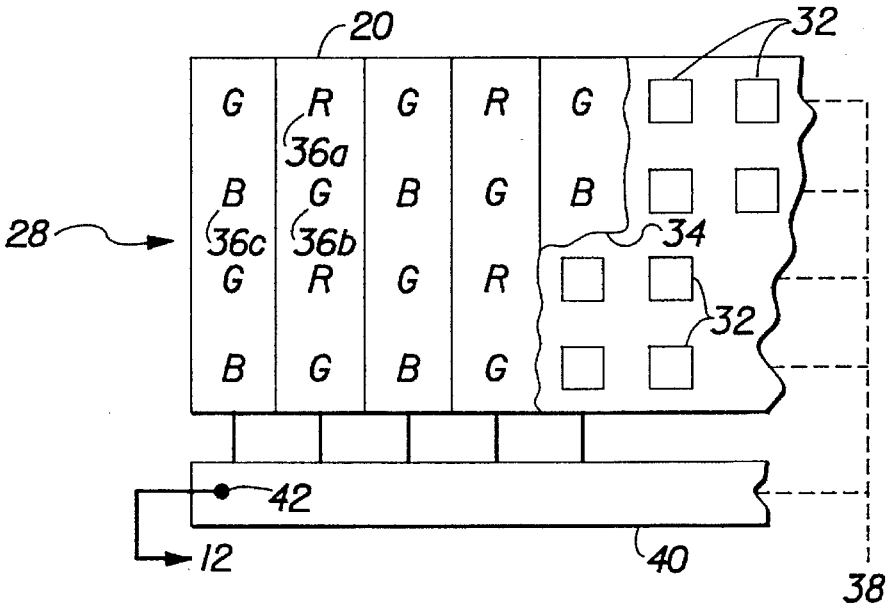

20
32
G
R
G
R
G
36a
B
G
B
G
B
28
36c
36b
34
G
R
G
R
32
B
G
B
G
42
12
40
38

FIG. 3

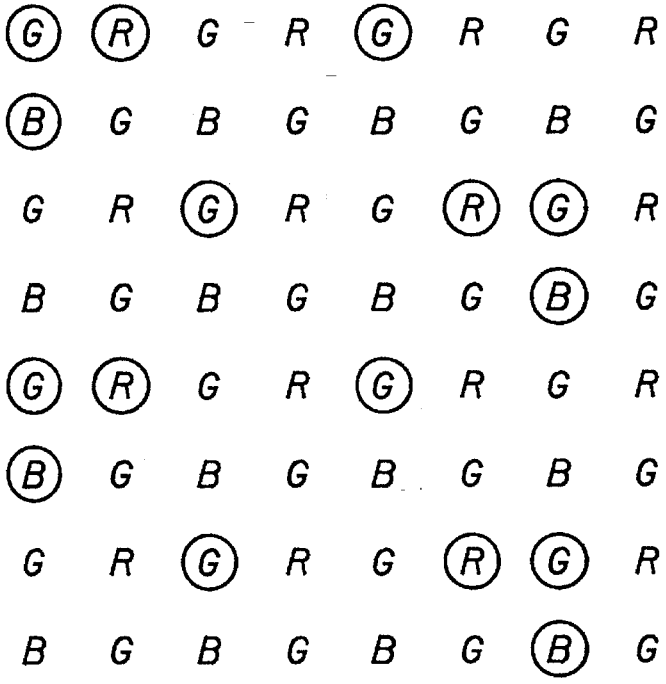

G R G R G R G R
B G B G B G B G
G R G R G R G R
B G B G B G B G
G R G R G R G R
B G B G B G B G
G R G R G R G R
B G B G B G B G

FIG. 4

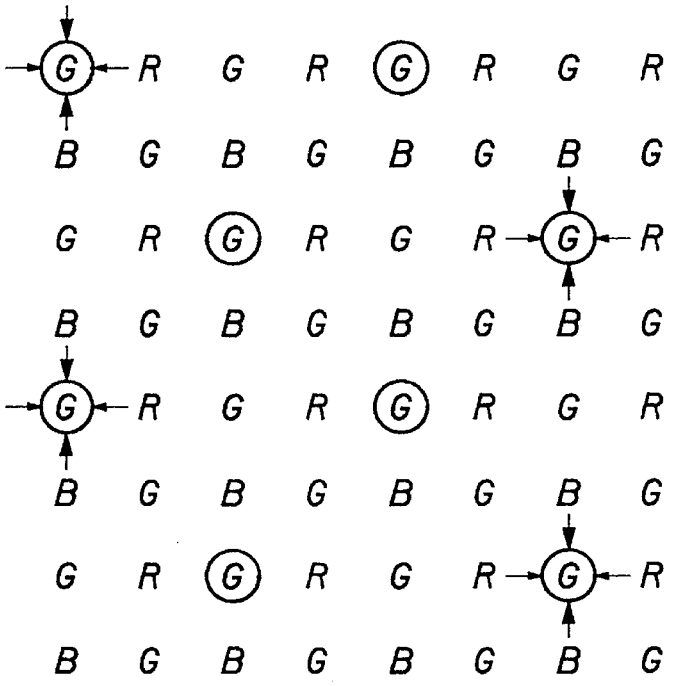

G R G R G R G R
B G B G B G B G
G R G R G R G R
B G B G B G B G
G R G R G R G R
B G B G B G B G
G R G R G R G R
B G B G B G B G

FIG. 5

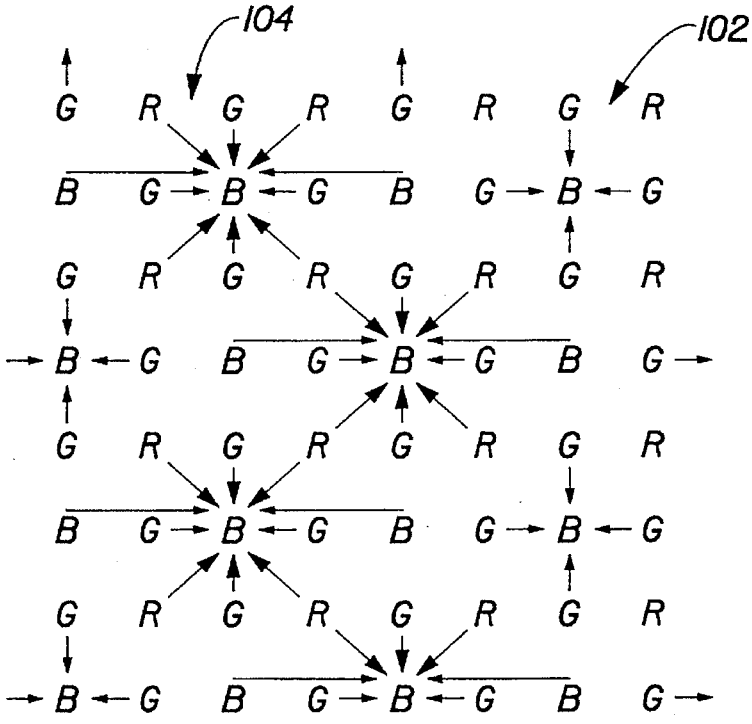

104
102
G R G R G R G R
B G B G B G B G
G R G R G R G R
B G B G B G B G
G R G R G R G R
B G B G B G B G
G R G R G R G R
B G B G B G B G

FIG. 6

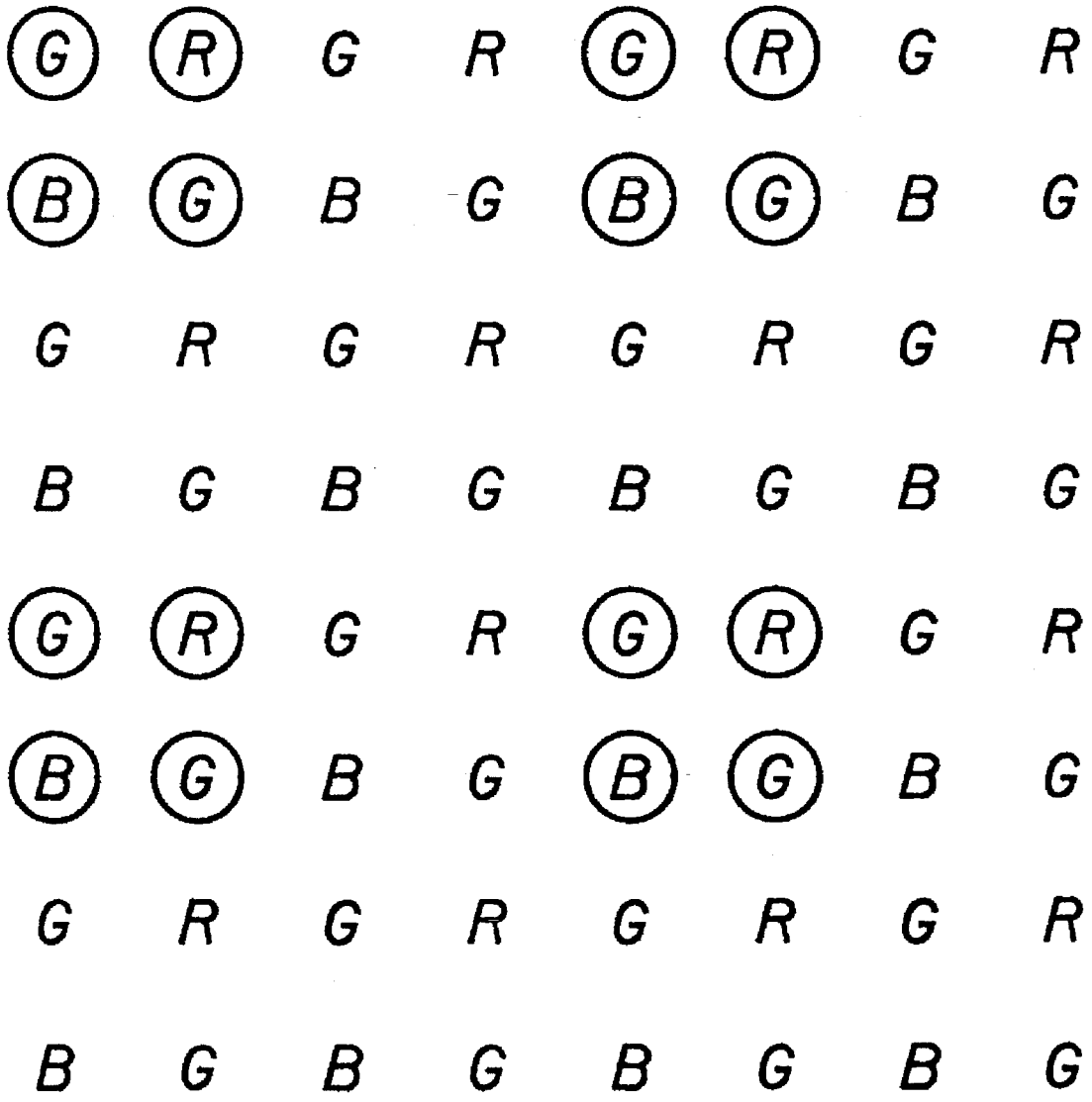

G R G R G R G R
B G B G B G B G
G R G R G R G R
B G B G B G B G
G R G R G R G R
B G B G B G B G
G R G R G R G R
B G B G B G B G

FIG. 7

# SINGLE SENSOR COLOR CAMERA WITH USER SELECTABLE IMAGE RECORD SIZE

## FIELD OF THE INVENTION

This invention relates to the field of electronic imaging and, in particular, to electronic still imaging by means of an electronic still camera having a single color sensor and semiconductor memory.

## BACKGROUND OF THE INVENTION

It is known in the prior art to provide an electronic camera with variable resolution modes by which the memory capacity required for recording an image can be changed as required, for example, to cope with limited residual memory in the recording medium.

U.S. Pat. No. 5,018,017 is representative of a camera utilizing such variability in resolution modes. The problem in the prior art, as set forth in this patent, is that provision of different resolution modes complicates the compatibility of removable memory used in electronic cameras. Whereas signal processing may be simple in construction when data corresponding to each picture element is simply recorded in the removable memory, any change in the number of filter elements or the arrangement of the color filter accordingly changes the arrangement of data recorded in the memory or the amount of data per image recorded in the memory. This means that the recorded memory cannot be interchangeably used with other camera systems having different sensor arrangements. While this problem is always a serious shortcoming, it becomes even more serious, and complicated, when several resolution modes are provided because each mode is likely to be dependent upon the particular color filter arrangement in use.

U.S. Pat. No. 5,018,017 solves this problem by preprocessing the baseband image data from the sensor, in this case to form luminance and color difference signals, before providing any change in resolution. This achieves a degree of uniformity, regardless of the sensor being used. Four resolution modes are provided, a full resolution mode and a lower resolution mode obtained by subsampling the full resolution signal, and two lesser resolution modes obtained by using progressively lower quantization levels in compressing the lower resolution image. In each case, the progressively lowered resolutions are derived from a color signal that is already preconverted into a standardized form. These reduced resolution modes offer more image storage for a given memory and open the possibility of continuously photographing, and recording, a series of images in memory that would, at full resolution, only store one, or a few, images. As noted in U.S. Pat. No. 5,018,017, the upper limit of the speed attained during such a burst mode is restricted by the time required for writing into the removable memory.

The principal shortcoming of known camera systems with several resolution modes is the amount of signal processing that is done between image capture and the point at which data reduction occurs. The more processing that occurs, the more chance for noise to enter the system before the new reduced resolution image is constructed. Moreover, a principal reason for going to reduced resolution in the first place is to free up memory storage for the taking, and storage, of more pictures. The camera is then able to load as many pictures as possible, and as quickly as possible, into the camera memory. However, the camera disclosed in this patent limits the attained speed to the access time to the removable memory, a circumstance that basically does not take full advantage of the reduced resolution modes. This is particularly the case where the removable memory is, as is usually the case, the slowest memory in the system.



Consequently, an object of the invention is to collapse the processing chain between image capture and resolution reduction so that problems caused by intervening processing are avoided.

Another object is to fully utilize the collapsed processing interval for continuous photography so that a subsequent circuit element, such as the removable memory, does not appreciably limit the attainable speed.

A further object is to permit the user to select an image record size in accordance with the need, whether for continuous photography or added storage for any other reason.

## SUMMARY OF THE INVENTION

In accordance with the invention, the aforementioned problems are solved with an electronic camera for processing images of different resolution, as set forth in the description of the preferred embodiments. As claimed, the camera includes an image sensor for generating a baseband image signal representative of color image pixels arranged in vertical and horizontal directions as obtained from a two-dimensional array of photosites covered by a pattern of luminance and chrominance color filters. A buffer memory includes sufficient capacity for storing the color image pixels as baseband signals corresponding to at least one image. An output memory, connected subsequent to the buffer memory, includes capacity for storing processed image signals obtained from the buffer memory. A resolution mode switch selects the pixel resolution of the image by specifying the order in which the color image pixels are selected for storage in both vertical and horizontal directions, the order including a full resolution mode in which all color image pixels are selected and at least one reduced resolution mode in which a fewer number of color image pixels are selected. A timing controller responsive to the pixel resolution selected by a resolution mode switch accordingly changes the number of horizontal and vertical pixels that represent the image by effecting a subsampling of the color image pixels for the reduced resolution mode. Finally, the selected color image pixels are stored in the output memory, such that the output memory is able to store more images in the reduced resolution mode than in the full resolution mode.

Several advantageous technical effects flow from the invention. One advantage is that each reduced resolution image directly corresponds to the image pixel data on the sensor, thus being a truer representation with less contamination by processing noise. Another advantage is that the processing channel before subsampling can be much simpler than in the prior art, with the usual attendant advantages in cost and speed. A further advantage is that the system can be designed to maximize incoming throughput into fast buffer memory, thus enhancing the speed of continuous photography. Other advantages and effects will become apparent in the ensuing description of the invention.

## BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be described in relation to the drawings, in which

FIG. 1 is a block diagram of a single sensor color camera with user selectable image record size in accordance with the invention;

FIG. **2** is a flowchart showing the operation of the camera shown in FIG. **1**;

FIG. **3** is a view of a portion of the sensor shown in FIG. **1**;

FIG. **4** is a view of the color pattern shown in FIG. **3** with an overlay of a first subsampling pattern;

FIG. **5** is a view of the color pattern shown in FIG. **3** with an overlay of a second subsampling pattern;

FIG. **6** is a view of the color pattern shown in FIG. **3** with an overlay of a third subsampling pattern; and

FIG. **7** is a view of the color pattern shown in FIG. **3** with an overlay of a fourth subsampling pattern.

## DESCRIPTION OF THE PREFERRED EMBODIMENTS

Since electronic still cameras employing a single color sensing device are well known, the present description will be directed in particular to elements forming part of, or cooperating more directly with, apparatus in accordance with the present invention. Elements not specifically shown or described herein may be selected from those known in the art.

Referring initially to FIG. **1**, the elements of a single sensor electronic camera are shown in block form. The camera is divided generally into an input section **10** for receiving image light and capturing an image, a processing and storage section **12** for processing and storing captured images, a control and display section **14** for user interface with the camera, and a detachable docking unit **16** for transferring stored images from the processing and storage section **12** to a host computer **18**. The camera shown in FIG. **1** is sometimes referred to as a dockable electronic still camera, since it relates to the computer **16** generally through a docking unit **16** (although, as will be described, a serial port is provided on the camera body itself for direct connection with the computer **18**).

The operation of the camera is generally shown in FIG. **2**. With this type of imaging system, the camera is generally removed from the docking unit **16** and used at a location significantly remote from the computer **18**. The camera is periodically returned to the computer, and images are then downloaded through the docking unit **16** (or the serial port) to free up the camera memory for more photographs. Because it is often inconvenient for the user to return to the computer to download images, the invention provides the user with the option to store some, or all, of the images at less than the highest resolution level, so that more images may be stored in the camera memory before having to return to the computer **18** to download the images. After the images are captured, the camera is connected to the docking adapter and the interface is initiated through the computer **18** (by appropriate software, which is not part of this invention). The desired images are selected, and perhaps previewed, through the computer **18**, and accordingly downloaded to its resident memory.

The input section **10** includes a lens **20** for imaging light from an object **22** through a shutter and aperture control **24** and an optical low pass filter **26** upon a charge-coupled device (CCD) image sensor **28**. The sensor **28** is shown in further detail in FIG. **3** to include a color filter array **30** overlying an array of photosites **32** (shown for illustration through a cutaway portion **34** of the color filter array **30**. The color filter array **30** has a plurality of red, green, and blue elements **36***a*, **36***b*, and **36***c* arranged in the familiar "Bayer array" described in U.S. Pat. No. 3,971,065, which is incorporated herein by reference. A characteristic of one form of the "Bayer array" is that the luminance picture elements (pixels), i.e., corresponding to the green element **36***b*, are arranged horizontally and vertically in a checkerboard pattern, and the chrominance pixels, i.e., corresponding to the red and blue color elements **36***a* and **36***c*, are each vertically and horizontally adjacent to a luminance pixel. A driver **38** (shown in FIG. **1**) generates clocking signals for controlling the image integration time and the vertical transfer of image pixels to a high speed horizontal register **40** (shown in FIG. **3**). An output capacitive node **42** produces a signal which is amplified, processed, and stored in the processing and storage section **12**.



Referring again to FIG. **1**, the input section further includes a lens cap **44** connected to a main switch **46** that activates the camera when the cap **44** is moved to expose the lens **20** to image light, and a close-up lens **48** that can be optionally moved into the path of image light for close-up exposures. The input section also includes an optical viewfinder **50** for framing the object **22** in relation to the sensor **28**, a flash unit **52** for illuminating the object **22**, and a photocell **54** for converting image intensity information into an electrical signal that is used in the processing and storage section **12** to regulate the shutter and aperture control **24**.

The processing and storage section **12** includes a correlated double sampling circuit **56** for providing analog image samples to a 10 bit analog-to-digital (A/D) converter **58**. The 10 bit digitized signals are corrected for white balance, gamma, and other conventional distortions by a correction read-only memory (ROM) **60**, which provides 8 bit output signals that are applied to a frame buffer memory **62**, which is a 4 megabit dynamic random-access memory (RAM). The buffered image signals are processed, e.g., compressed, in a digital signal processor (DSP) **64** and then stored in an output memory, such as flash electrically programmable read-only memory (EPROM) **66**. When the camera is to send image data to the computer **18**, one of two data paths are used. A serial path from the flash EPROM memory **66** to a serial port **68** is provided through a universal synchronous/asynchronous receiver/transmitter (UART) **70** and an RS232 driver **72**. Alternatively, a faster parallel path is provided through connectors **74***a* and **74***b* via a small computer systems interface (SCSI) controller **76** in the docking unit **16** to a parallel port **78**.

A timing generator **80** provides timing signals to the aforementioned elements in the processing and storage section **12**, in particular providing timing input to an 8-bit microprocessor controller **82** and address timing to the frame buffer memory **62**, the DSP **64**, the flash EPROM memory **66**, and a latching and decoding circuit **84**. The microprocessor controller in turn controls the A/D converter **58**, the correction ROM **60**, the flash unit **52**, and a stepping motor driver **86**, which controls operation of the shutter and aperture control **24**. The microprocessor controller **82** also controls a display element **50***a* in the viewfinder **50** (for indicating flash ready, under/over exposure, and the like), and receives exposure data from the photocell **54**.

While the processing and storage section **12** automatically controls image exposure upon the CCD sensor **28** by means of data input from the photocell **54**, a plurality of switches are provided in the control and display section **14** for manually activating a variety of additional features. (Some switches directly activate the respective features, while other switches activate a menu of choices on a liquid crystal display (LCD) **90**.) For instance, a switch **88***a* moves the close-up lens **48** into position, a switch **88***b* allows the user

to select which of two (high or low) different resolution levels of sensor data are stored in the frame buffer memory **62**, a switch **88***c* activates a low resolution "burst" mode in which several pictures are rapidly taken, a switch **88***d* activates the flash unit **52**, and a switch **88***e* activates a self-timer delay mode. A capture switch **88***f* initiates each exposure. The liquid crystal display (LCD) **90** indicates the selected feature values. Depending upon the capabilities of the camera, further input may be provided, e.g., levels of compression (number of bits) may be selected, and the color mode (black/white or color) may be designated.

A battery **92** provides power to the camera through a power switcher **94** and a DC/DC converter **96** when the camera is disconnected from the docking unit **16**. When the docking unit **16** is connected between the computer **18** and the camera, the computer supplies power to an AC/DC converter **98** in the docking unit **16**, which in turns powers a battery charger **100** that connects to the camera and charges the battery **92**.

In using the camera according to the invention, activation of the capture switch **88***f* allows the camera to capture one or a plurality of images, which are then stored in the flash EPROM memory **66**, until they can be downloaded to the computer **18**. The image which is read out from the sensor **28** has, in one embodiment, a total of 512 lines and 768 pixels per line. Since the sensor **28** incorporates a "Bayer" color filter pattern, the digitized values from the A/D converter **58** correspond to values from the various color elements **36***a*, **36***b*, **36***c* on the sensor **28**. Eight bit digital pixel values are read from the CCD sensor **28** via ROM **60** at a **2** MHz readout rate and stored in the 4 megabit dynamic RAM frame buffer memory **62**. About 200 msec are required to read one image from the sensor **28**, and into the frame buffer memory **62**. The image signals are then read from the frame buffer memory **62** at a slower speed, compressed using a DPCM algorithm (which compresses the image from 8 bits per pixel to 2 bits per pixel) implemented in the DSP **64** pursuant to instructions stored in a program ROM **64***a*, and stored in the flash EPROM memory **66**, which can hold several compressed images. This process takes about 4 seconds, which means that full resolution images can only be stored in the flash EPROM memory **66** every 4 seconds. The use of the buffer memory **62** allows the DSP **64** to operate at a throughput rate different from the CCD sensor **28**, as described in U.S. Pat. No. 5,016,107, entitled, "Electronic Still Camera Utilizing Image Compression and Digital Storage", which is incorporated herein by reference. The aforementioned latching and decoding circuit **84** accomplishes this separation of throughput rates by coordinating the requirement of the DSP **64** with control of the frame buffer memory **62** and the flash EPROM memory **66**.

According to the invention, the camera includes the switch **88***b* which allows the user to select the image record size, that is, which of two different resolution levels of sensor data are stored in the frame buffer memory **62**. When the switch **88***b* activates the "low resolution" mode, the timing generator **80** changes the timing to the buffer memory **62** so that, in one embodiment, only a quarter of the pixels on the CCD sensor **28** are stored in the memory **62**. This quarter size image is then compressed by the DSP **64**, and stored in the flash EPROM memory **66**. It is thus possible to store four times as many low resolution images as high resolution images in the flash memory **66**. In addition, it is possible to store up to five low resolution images rapidly into the buffer memory **62**. Consequently, when the user holds down the capture switch **88***b*, with the burst mode enabled by actuation of the switch **88***c*, a burst of up to five low resolution images is taken in rapid succession. These images are then read out, one by one, compressed, and stored in the flash EPROM memory **66**.

In order to form the low resolution images, a suitable "subsampling" pattern is required. For example, if only every second pixel of every second line was selected for storage in the buffer memory, the image would contain only values of one of the three colors. To provide a color image, the color filter array pixels must be subsampled properly. This subsampling should be done in a manner that maintains good luminance resolution, without introducing false color "aliasing" artifacts. One subsampling pattern is shown in FIG. **4**, with a circle surrounding each sampled pixel. In this pattern, the green (luminance) elements are subsampled in a checkerboard type arrangement, by selecting every second green element of every second line, but staggering the sampling by one element to form a "subsampled Bayer type checkerboard". The red and blue elements near the selected green elements are chosen in order to provide color samples which are spatially adjacent with at least some of the luminance samples. This minimizes the false color edges which might otherwise occur.

In alternate subsampling patterns, the image is stored in the frame buffer memory **62** in the low resolution mode, and the DSP **64** processes the values from multiple pixels of the same color to form the color subsampled image, by averaging some of the pixels. One such pattern is shown in FIG. **5**, with the (unaveraged) pixels surrounded by a circle and the averaged pixels at the base of respective arrows. Here, the green pixel values are used directly, while the two horizontally adjacent red values are averaged (as schematically shown by arrows) to form a red pixel value at every second green location, and the two vertically adjacent blue values are averaged (as shown by the arrows) to from a blue pixel value at the same locations. Green is not averaged, in order to maintain higher resolution. Unfortunately, this arrangement can cause some luminance aliasing. A further pattern, shown in FIG. **6**, also averages the green values to eliminate this luminance aliasing. This averaging, however, also reduces the image sharpness. In FIG. **6**, the 4 nearest green pixels in a "cross" shaped pattern in a first group **102** are averaged (as shown by the arrows). For every second group **104** of four green pixels, the four nearest red pixels are averaged, and one-half the value of the center blue pixel is summed with one-half the average value of the two horizontally adjacent blue elements. In all cases (FIGS. **4–6**) the subsampling always maintains a ratio of two green pixel values, for every red or blue pixel value.

The subsampling illustrated by FIG. **4** is obtained by suitably programming the microprocessor controller **82** to instruct the timing generator **80** to produce address and control signals at the proper intervals so as to store only the values of the circled pixels of FIG. **4** into frame memory **62**. The values from the non-circled pixels are not stored. The subsampling patterns illustrated by FIG. **5** and **6** are obtained by suitably programming the microprocessor controller **82** to instruct the timing generator **80** to produce address and control signals so as to store the pixel values which are either circled or at the tails of the arrows, in the respective figures.

Because only a fraction of the pixel values on the sensor **28** are stored for any of the subsampling modes shown in FIGS. **4–6**, the frame memory **62** is sufficient to store multiple images. When the burst mode controlled by switch **88***c* is enabled, the microprocessor controller **82** instructs the timing generator to capture a burst of low resolution images and store the subsampled pixel values of each low resolution image in successive address areas of frame memory **62**.

Because the subsampling pattern shown in FIG. **4** allows a smaller number of pixels to be stored in frame memory **62**, it has, compared to the patterns shown in FIGS. **5–6**, the advantage of allowing bursts containing a larger number of low resolution images to be captured at a relatively fast rate (approximately two frames per second) instead of at the slow rate (approximately four seconds per frame) of the high resolution mode, which is limited by the speed of flash memory **66** and DSP processor **64**. In all cases, the requisite programming of the microprocessor controller **82** and the timing generator **80** is well within the talents of a programmer possessing the ordinary skills of this art. Other subsampling patterns may be useful; preferably these would also include chrominance elements (red or blue) spatially adjacent to luminance elements (green). Other filter arrays, and patterns, may be used, e.g., based on complementary colors (cyan, magenta, and yellow).

Sometimes a simplified version of the invention is preferred where the main advantage sought is the increased storage space, rather than a burst mode capability. A preferred "quarter size" subsampling pattern for such usage is shown in FIG. **7**, with a circle surrounding each sampled pixel. In this case, all of the digitized image is stored in the frame memory **62**. Clocking is thus simplified for the buffer memory **62** because only one clock, rather than two, is required. Then, the DSP **64** decimates the original pixels and generates a "quarter size" Bayer pattern image, as shown in FIG. **7**. Because the DSP **64** is designed to be programmable, it is less difficult to have the DSP **64** do the "subsampling" than to specially program the clock for the buffer memory **62** to do the same.

The invention has been described in detail with particular reference to a preferred embodiment thereof, but it will be understood that variations and modifications can be effected within the spirit and scope of the invention. For example, while two resolution modes are disclosed in connection with the camera of FIG. **1**, the same principles apply regardless of the number of modes. For instance, a third mode could further subsample the pattern of sampled elements shown in FIG. **4** to provide a yet lower resolution image.

PARTS LIST

| | |
|---|---|
| 10 | INPUT SECTION |
| 12 | PROCESSING AND STORAGE SECTION |
| 14 | CONTROL AND DISPLAY SECTION |
| 16 | DETACHABLE DOCKING UNIT |
| 18 | HOST COMPUTER |
| 20 | LENS |
| 22 | OBJECT |
| 24 | SHUTTER AND APERTURE CONTROL |
| 26 | OPTICAL LOW PASS FILTER |
| 28 | CCD IMAGE SENSOR |
| 30 | COLOR FILTER ARRAY |
| 32 | PHOTOSITES |
| 34 | CUT-AWAY PORTION OF THE SENSOR |
| 36A | RED COLOR ELEMENT |
| 36B | GREEN COLOR ELEMENT |
| 36C | BLUE COLOR ELEMENT |
| 38 | DRIVER |
| 40 | HORIZONTAL REGISTER |
| 42 | OUTPUT CAPACITATIVE NODE |
| 44 | LENS CAP |
| 46 | MAIN SWITCH |
| 48 | CLOSE-UP LENS |
| 50 | OPTICAL VIEWFINDER |
| 52 | FLASH UNIT |
| 54 | PHOTOCELL |
| 56 | CORRELATED DOUBLE SAMPLING CIRCUIT |
| 58 | A/D CONVERTER |
| 60 | CORRECTION ROM |

-continued

PARTS LIST

| | |
|---|---|
| 62 | FRAME BUFFER MEMORY |
| 64 | DSP |
| 64A | PROGRAM ROM |
| 66 | FLASH EPROM MEMORY |
| 68 | SERIAL PORT |
| 70 | UART |
| 72 | RS232 DRIVER |
| 74A | CONNECTOR |
| 74B | CONNECTOR |
| 76 | SCSI CONTROLLER |
| 78 | PARALLEL PORT |
| 80 | TIMING GENERATOR |
| 82 | MICROPROCESSOR CONTROLLER |
| 84 | LATCHING AND DECODING CIRCUIT |
| 86 | STEPPING MOTOR DRIVER |
| 88A | CLOSE-UP SWITCH |
| 88B | RESOLUTION SWITCH |
| 88C | BURST MODE SWITCH |
| 88D | FLASH SWITCH |
| 88E | SELF-TIMER SWITCH |
| 88F | CAPTURE SWITCH |
| 90 | LCD |
| 92 | BATTERY |
| 94 | POWER SWITCHER |
| 96 | DC/DC CONVERTER |
| 98 | AC/DC CONVERTER |
| 100 | BATTERY CHARGER |
| 102 | FIRST GROUP |
| 104 | SECOND GROUP |

What is claimed is:

**1**. An electronic camera adapted for processing images of different resolution, said camera comprising:

an image sensor for generating a baseband image signal representative of color image pixels arranged in vertical and horizontal directions as obtained from a two-dimensional array of photosites covered by a pattern of luminance and chrominance color filters;

a buffer memory having sufficient capacity for storing the color image pixels as baseband signals corresponding to at least one image;

an output memory, connected subsequent to the buffer memory, for storing processed image signals obtained from the buffer memory;

a resolution mode switch for selecting a pixel resolution of the image by specifying an order in which the color image pixels are selected for storage in both vertical and horizontal directions, said order including a full resolution mode in which all color image pixels are selected and at least one reduced resolution mode in which less than all color image pixels are selected;

a controller responsive to the pixel resolution selected by the resolution mode switch for accordingly changing the number of horizontal and vertical pixels that represent the image, said controller effecting a subsampling of the color image pixels for the reduced resolution mode; and

means for storing the selected color image pixels in said output memory, whereby said output memory is able to store more images in said reduced resolution mode than in said full resolution mode.

**2**. A camera as claimed in claim **1** in which said storing means stores a plurality of different resolution images in said output memory, depending on the resolution mode selected by said resolution mode switch for each image.

**3**. A camera as claimed in claim **1** in which said buffer memory is operable according to a timing signal that regulates the order in which the color image pixels are selected for storage in said buffer memory, and said controller

responsive to the selected pixel resolution generates the timing signal and accordingly effects the subsampling by selecting appropriate pixels for storage in said buffer memory.

**4**. A camera as claimed in claim **1** wherein said controller further enables a burst mode wherein a multiplicity of subsampled images are stored in said buffer memory, and wherein said storing means subsequently transfers said subsampled images to said output memory.

**5**. A camera as claimed in claim **1** wherein said buffer memory is operable to store all of the color image pixels from said image sensor as baseband signals, and wherein said controller effectuates the subsampling for the selected pixel resolution by accordingly selecting appropriate pixels from said buffer memory for storage in said output memory.

**6**. A camera as claimed in claim **4** wherein said controller further averages certain of the selected pixels before storage in said output memory.

**7**. An electronic camera adapted for processing images of different resolution, said camera comprising:

an image sensor for generating a baseband image signal representative of color image pixels arranged in vertical and horizontal directions as obtained from a two-dimensional array of photosites covered by a pattern of luminance and chrominance color filters;

a buffer member having sufficient capacity for storing the color image pixels as baseband signals corresponding to at least one image, said memory operable according to a timing signal that regulates the order in which the color image pixels are selected for storage in said buffer memory;

a resolution mode switch for selecting a pixel resolution of the stored image by specifying an order in which the color image pixels are selected for storage in both vertical and horizontal directions, said order including a full resolution mode in which all color image pixels are stored and at least one reduced resolution mode in which a fewer number of color image pixels are stored; and

a timing controller responsive to the pixel resolution selected by the resolution mode switch for generating the timing signal and accordingly changing the number of horizontal and vertical pixels that represent the image, said timing signal effecting a subsampling of the color image pixels for the reduced resolution mode wherein each chrominance image pixel is selected to be spatially adjacent to a selected luminance image pixel.

**8**. An electronic camera adapted for processing images of different resolution, said camera comprising:

an image sensor for generating a baseband image signal representative of color image pixels arranged in vertical and horizontal directions as obtained from a two-dimensional array of photosites covered by a pattern of luminance and chrominance color filters;

a buffer memory having sufficient capacity for storing the color image pixels as baseband signals corresponding to at least one image, said memory operable according to a timing signal that regulates the order in which the color image pixels are selected for storage in said buffer memory;

a resolution mode switch for selecting a pixel resolution of the stored image by specifying an order in which the color image pixels are selected for storage in both vertical and horizontal directions, said order including a full resolution mode in which all color image pixels are stored and at least one reduced resolution mode in which less than all color image pixels are stored; and

a timing controlling responsive to the pixel resolution selected by the resolution mode switch for generating the timing signal and accordingly changing the number of horizontal and vertical pixels that represent the image, said timing signal effecting a subsampling of the color image pixels for the reduced resolution mode wherein (a) the luminance image pixels are subsampled in a checkerboard-type arrangement and (b) the chrominance image pixels are subsampled so as to be spatially adjacent to a luminance image pixel.

**9**. An electronic camera adapted for processing images of different resolution, said camera comprising:

an image sensor for generating a baseband image signal representative of color image pixels arranged in vertical and horizontal directions as obtained from a two-dimensional array of photosites covered by a pattern of luminance and chrominance color filters;

a buffer memory having sufficient capacity for storing the color image pixels as baseband signals corresponding to at least one image, said buffer memory operable according to a timing signal that regulates the order in which the color image pixels are selected for storage in said buffer memory;

a resolution mode switch for selecting a pixel resolution of the stored image by specifying an order in which the color image pixels are selected for storage in both vertical and horizontal directions, said order including a full resolution mode in which all color image pixels are stored and at least one reduced resolution mode in which less than all color image pixels are stored;

a timing controller responsive to the pixel resolution selected by the resolution mode switch for generating the timing signal and accordingly changing the number of horizontal and vertical pixels that represent the image, said timing signal effecting a subsampling of the color image pixels for the reduced resolution mode wherein each chrominance image pixel is selected to be spatially adjacent to a luminance image pixel;

a signal processor for generating a processed image signal by compressing the baseband image signal stored in said buffer memory; and

an output memory having sufficient capacity for storing the processed image signal corresponding to at least one full resolution image, or to a greater number of reduced resolution images.

**10**. A camera as claimed in claim **9** in which said output memory stores a combination of said full resolution and reduced resolution images, depending on the resolution mode selected by said resolution mode switch for each image.

**11**. An electronic camera adapted for processing images of different resolution, said camera comprising:

an image sensor for generating a baseband image signal representative of color image pixels arranged in vertical and horizontal directions as obtained from a two-dimensional array of photosites covered by a pattern of luminance and chrominance color filters;

means for exposing said image sensor to image light from at least one image;

a buffer memory having sufficient capacity for storing the color image pixels as baseband signals corresponding to at least one image, said buffer memory operable according to a timing signal that regulates the order in which the color image pixels are selected for storage in said buffer memory;

a resolution mode switch for selecting a pixel resolution of the stored image by specifying an order in which the

color image pixels are selected for storage in both vertical and horizontal directions, said order including a full resolution mode in which all color image pixels are stored and at least one reduced resolution mode in which less than all color image pixels are stored;

a timing controller responsive to the pixel resolution selected by the resolution mode switch for generating the timing signal and accordingly changing the number of horizontal and vertical pixels that represent the image, said timing signal effecting a subsampling of the color image pixels for the reduced resolution mode wherein each chrominance image pixel is selected to be spatially adjacent to a luminance image pixel;

a signal processor for generating a processed image signal by compressing the baseband image signal stored in said buffer memory;

an output memory having sufficient capacity for storing the processed image signal corresponding to at least one full resolution image, or to a greater number of reduced resolution images; and

means responsive to the reduced resolution mode selected by said resolution mode switch for enabling said exposing means to continuously expose said sensor to a series of images, whereby a corresponding series of processed image signals are generated by said signal processor and stored in said output memory.

**12**. An electronic camera adapted for processing images of different resolution, said camera comprising:

an image sensor for generating a baseband image signal representative of color image pixels arranged in vertical and horizontal directions as obtained from a two-dimensional array of photosites covered by a checkerboard pattern of luminance and chrominance color filters in which each luminance image pixel is horizontally and vertically adjoined by a chrominance image pixel;

a buffer memory having sufficient capacity for storing the color image pixels as baseband signals corresponding to at least one image;

a signal processor for generating a processed image signal by compressing the baseband image signal stored in said buffer memory; and

a resolution mode switch for selecting a pixel resolution mode of the image selected for compression, said resolution modes including a full resolution mode in which all color image pixels are processed for compression and at least one reduced resolution mode in which less than all color image pixels are produced by averaging at least some of the color image pixels before compression.

**13**. A camera as claimed in claim **12** in which the fewer number of color image pixels produced in the reduced resolution mode include a subsampled array of luminance image pixels and averaged values of the chrominance image pixels horizontally and vertically adjacent to at least some of the subsampled luminance image pixels.

**14**. A camera as claimed in claim **12** in which the fewer number of color image pixels produced in the reduced resolution mode include averages of luminance image pixels both horizontally and vertically adjacent to an array of chrominance image pixels.

**15**. A camera as claimed in claim **12** in which the fewer number of color image pixels produced in the reduced resolution mode represent luminance and chrominance values that are averaged over an array of positions that are adjacent to an array of chrominance image pixels.

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